STUDIES ON LOW VOLTAGE-LOW POWER MOS DEVICES FOR DIGITAL INTEGRATED CIRCUITS(Dissertation_全文)

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Final Report

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LIST OF SYMBOLS

C	capacitance
C_{OX}, C_O	oxide capacitance
C_D	Debye capacitance
E	field
E_X	field perpendicular to the surface
E_y	field toward source-to-drain direction
E_s	surface field
E_c	critical field
E_{sO}	$= 6 \times 10^4$ V/m
f	frequency
h	mesh size
J	current density
I	current
I_D	drain current
k	Boltzmann's constant
K	substrate back-bias constant
L	channel length
L_E	enhancement region channel length
L_T	total channel length
L_{eff}	effective channel length
L_{DI}	intrinsic Debye length
N	doping density, electron density
N_{ss}	surface state density
N_A	acceptor density
N_D	donor density
N_I	intrinsic carrier density
N_{IMPL}	implanted impurity density
N_r	$= 6.3 \times 10^{16}$ cm^{-3}
N_{DT}	total implanted dose/cm^{-2}

P_{ON}	on-power
q	electron charge
Q_N	induced electron charge
Q_{SF}	total surface charge
Q_B	bulk charge
R	resistance
r_{ON}	on-resistance of MOSFET
R_M	projected range of implanted ions
T_{OX}	oxide thickness
T	temperature
U	voltage or potential in the (kT/q) unit
U_G	gate voltage
U_D	drain voltage
U_S	source voltage
U_F	Fermi potential
U_{SF}	surface potential
U_{S1}	$U_{S3} - U_S$
U_{S2}	surface potential at the pinch-off point
U_{S3}	surface potential at the source
U_{DS}	saturation drain voltage
U_T	threshold voltage
V	voltage
v	voltage normallized by the supply voltage
v	velocity of carriers
v_{sat}	saturation velocity of carriers
V_{GG}	gate voltage of the load device
V_{DD}	supply voltage
V_{ON}	on-level
V_{BB}	back-bias voltage
V_T	threshold voltage
V_G	gate voltage
V_S	source voltage
V_D	drain voltage

V_{DS}	saturation drain voltage
V_{FB}	flat-band voltage
ΔV_G	gate voltage variation that corresponds to one decade variation of the drain current in the tail current region of MOSFET
V_{OFF}	off-level
V_{c1}	high-level circuit threshold
V_{c2}	low-level circuit threshold
V_{m1}	high-level margin
V_{m2}	low-level margin
W	width of the channel
t_d	delay time
$t_{1/2}$	time needed for the output node to be charged from low to a half of the supply voltage
x	distance toward the direction perpendicular to the surface measured from the surface
x_s	depth of the pinch-off region
x_c	depth of the channel region at the pinchoff point
x_D	depth of the drain diffusion
y	distance toward the source-to-drain direction measured from the source
y_{po}	pinch-off point
β	channel conductance constant of MOSFET
β_0	low gate field channel conductance
β_D	channel conductance constant of driver transistor
β_L	channel conductance constant of load transistor
β_R	driver/load channel conductance ratio
ϵ_S	dielectric constant of silicon
ϵ_{OX}	dielectric constant of oxide
γ	C_D/C_0 ratio
ξ	quasi-Fermi potential in the unit of (kT/q) measured from bulk Fermi level

$\sigma, \sigma_1, \sigma_2$	standard deviations
ϕ_M	work function of gate metal or semiconductor
ϕ_{MS}	work function difference between the gate and the silicon
ϕ_F	Fermi potential
χ	electron affinity of silicon
μ	mobility of carriers
μ_0	low gate-field mobility
μ_{max}	mobility at low doping limit
μ_{min}	mobility at high doping limit
θ	constant that expresses the gate field dependence of mobility (m/V)
θ_a	constant that expresses the gate voltage dependence of mobility (V^{-1})
ω	over-relaxation constant

ABSTRACT

In this thesis, MOSFET models and analyses for low voltage MOS integrated circuits, properties of enhancement-depletion (E/D) static and dynamic circuits, and a new CMOS process are studied. The major purpose of this study is to solve power dissipation problems that will limit the integration density in a very large scale circuit. A number of models and analyses in this thesis aim to provide convenient design tools for more advanced designs.

An accurate and practical model for standard MOSFET that applies over a wide range of current including the subthreshold region is developed. The model utilizes analytical current equations divided into three operation regions for the MOSFET: the non-saturation region, the saturation region and the tail current region. The equations are derived based on an accurate calculation of the surface potentials at the source end of the channel and at the pinch-off point. The comparison of the current-voltage characteristics between theory and experiments for a wide range of oxide thicknesses, substrate doping densities and temperatures indicates the agreement is excellent in a current range 10^{-2} to 10^{-11} A.

Threshold voltage control and low-level current control in MOSFET by ion-implantation is discussed. It is shown that a single layer implantation has some limitations in a low voltage circuits because the characteristics of the transistors at low currents are strongly influenced by the implantation condition. It is proposed that a double-layer implantation provides a great flexibility in controlling the low-level currents. For instance, the double-layer implantation of differing species makes possible a nearly parallel shift of the log $I_D - V_G$ curves. It also realizes MOSFETs having residual currents and MOSFETs having less steep log $I_D - V_G$ curves depending on the condition. These features are realized independent of the control of the threshold voltage.

The double-diffused MOSFET realizes effectively short channel device without suffering from a number of short channel effects. A numerical analysis of the double-diffused MOSFET that is based on accurate charge equations and dependence of mobility on gate and drain field and doping is carried out. The gradient of doping along the channel plays an important role to determine the current versus voltage characteristics. Both symmetrical and asymmetrical doping profiles are analyzed through this study.

Design and experiments of enhancement/ depletion (E/D) circuits are discussed. A general design approach for static inverters for the purpose of optimizing the dc-transfer curves is proposed with an emphasis on the operation at five volts and at 1.5 volts. Dynamic operation of the E/D configuration is proposed for address circuits in random-access memories. Based on these design theories and circuit techniques, a prototype read-only memory and a random-access memory are designed and are successfully operated with a single +5-volt supply. Enhancement type MOSFET with Al_2O_3/ SiO_2 double layer gate insulator and depletion type MOSFET with PSG/SiO_2 double layer are integrated on a same chip.

Complementary MOS (CMOS) technology is most suitable for low power applications because of its zero quiescent current. However, the complex process results in a low yield and low circuit density. A new simplified CMOS process that utilizes a symmetrical double-diffused MOSFET for the n-channel device is proposed. The features of the new technology are; the use of five masks that is simpler than any existing technologies and the avoidance of the need to align the p-well to the source and the drain diffusions of n-channel devices. This results in a fifty percent reduction of the cell size as compared to conventional CMOS processes. A detailed analysis of the n-channel symmetrical DMOSFET in the CMOS cell is also discussed.

CHAPTER 1 INTRODUCTION

The concept of a "field-effect transistor" was first introduced by Lilienfeld [1] in 1930, and by Heil [2] in 1935 independently. This indicates that the field-effect transistor is a rather old device. However, practical field-effect transistors did not appear for quite a long time because of difficulties in controlling the surface properties of semiconductor crystals. In 1960, Kahng and Attala [3] - [5] first proposed the Metal-Oxide-Semiconductor field-effect transistor (MOSFET) in essentially its present form. In ensuing years, much work has been devoted to understanding the Si-SiO_2 interface and behavior of MOSFETs. In 1963, the first MOS integrated circuit appeared, [6] and it was demonstrated that the MOSFET has potential advantages in the application to large scale integration. The major advantageous features of the MOSFET are:

(1) MOSFETs are self-isolated and occupy a relatively small surface area.

(2) Large input resistance of MOSFET makes possible the use of dynamic circuits that is effective in reducing the number of transistors.

(3) The threshold voltage of MOSFETs can be adjusted both positively and negatively by various processing modifications.

There has been very rapid progress in the number of MOSFETs integrated on a chip. Until recently, the rate of growth was a doubling in every year. Recent integrated circuits (in 1976) contain more than 20,000 transistors. It is obvious that if this tendency continues, the power dissipation of the circuit will increase, and finally, the integration density will reach a limit determined by the maximum power allowed.

The power dissipation of the circuit is basically limited by the junction temperatures attained. This, in turn, is determined by the thermal resistance of silicon and the package, and by the

ambient temperature. This limitation is about one watt in a practical plastic or ceramic package. Thus, the reduction of the power per unit cell is strongly required in order to increase the integration density.

A power consumption of an ideal complementary inverter circuit that consists of a switch to charge the capacitance at the output node to a high level when the input is low, and a switch to discharge the capacitance when the input is high, is given by $CV_{DD}^2 f$, where V_{DD} is the supply voltage and f is the operating frequency. This means that both the supply voltage and the capacitance should be decreased in order to reduce the power dissipation. Much effort is now being made to reduce the capacitance by shrinking device sizes and line widths. [7] Because of the square law current dependence on gate voltage, the reduction of the operating voltage would be even more effective way. In standard logic or memory circuits, a single five-volt supply appears to be most convenient because a typical bipolar circuit family (TTL) is operated with a five-volt supply. Compatibility with TTL is of great importance in building systems. There are, however, some special applications that need very low power dissipation. A typical example for this is complementary MOS (CMOS) integrated circuits for use in electronic wrist watches [8], and other micropower applications that usually are operated with 1.3 to 1.5-volt supply.

Low-voltage operation of MOSFET circuits, has stimulated the necessity to rebuild an overall design, analysis and fabrication of MOS integrated circuits and to solve a number of problems associated with the low-voltage operation. These include, device design and modelling of low-threshold MOSFETs, threshold control techniques, control of low-level currents, low-voltage oriented MOS circuit design and circuit innovations, and the development of new processes.

This thesis studies device, circuit and processing innovations in low voltage and low power MOS integrated circuits. The background for this research will be discussed first in Chapter 2. Power limitations in large scale integrated circuit is a special focus of that discussion. Some of the efforts to reduce power of the unit cell that have been tried so far will be reviewed. A simple power comparison for several types of digital circuits and a discussion on the control of threshold voltage will be made in this chapter.

Chapter 3 presents a number of MOSFET models and analyses for low voltage applications. One of the problems that circuit designers encounter in low voltage circuits is the subthreshold drain currents in MOSFETs. In simple models, these currents are neglected, but this is not accurate. Thus, a new model of MOSFET, that expresses the dc-behavior of MOSFET from 10 pA to the typical one or more mA level that is handled by simple models, is proposed, and the results of extensive comparison with measurements will be shown. The study is then extended to analysis and experiments concerned with subthreshold currents in ion-implanted MOSFETs. The control of the subthreshold currents by employing succesively two different implantations will also be proposed. This process makes possible a control of low-level currents that is independent from the control of the threshold voltage.

Another problem in low voltage circuit is that the transconductance of the transistors falls off when the gate bias is low. A useful device in such a case is a double-diffused MOSFET. The double-diffused MOSFETs have a non-uniform doping toward the source-to-drain direction, and do not obey the equations used for standard MOSFETs. The last section in Chapter 3 deals with a precise one-dimensional analysis of the double-diffused MOSFET. Current-voltage relationships and field and potential distributions in the device will be studied through the analysis. This analysis enables a careful comparison of both asymmetrical and symmetrical doping

profiles.

In Chapter 4, the design and experiments of Enhancement/Depletion (E/D) circuits are studied. First, the design theory of the E/D type static inverter circuit will be discussed. The design is based on maximizing the noise margins of the circuit. A general design approach that is applicable to any operating voltage and some design examples for supplies ranging from five volts down to 1.5 volts will be shown. Second, dynamic operation of E/D circuits is proposed for addressing circuits in random-access memories. The purpose for this is to propose address circuitry for +5-volt single supply dynamic random-access memories, and to discuss problems that are inherent in the dynamic and low voltage operation of MOS circuits.

In MOS integrated circuits, minimum quiscent power has so far been obtained in complementary MOS circuits. Thus, this technology appears to be important in the future large scale integration. However, the drawback of the CMOS is that it requires a very complex process and the density of the circuit is low. In Chapter 5, a new CMOS process that features a simpler process and denser integration density than conventional CMOS will be proposed. The results of measurements on sample devices and circuits in this new CMOS process will be shown.

Overall conclusions and the suggestions for further study are contained in Chapter 6.

CHAPTER 2 POWER CONSIDERATIONS IN DIGITAL MOS CIRCUITS

2.1 Large Scale Integration and Power

Power dissipation in digital MOS integrated circuits is determined by several factors. First of all, power dissipation depends upon types of circuits, and processing technologies. For instance, the choices of p, n-channel devices or complementary MOS, static or dynamic circuit, enhancement-load or depletion load, determine the power dissipation. Second factor is the supply voltage. A simple calculation of the power dissipation and the delay time for any of these circuits, as will be revealed in the next Section, leads to the fact that the power-delay product is in proportion to (capacitance at the output node) × (supply voltage)^2. This clearly illustrates that one of the effective ways to reduce power while keeping the delay time constant, is to decrease the supply voltage. This also indicates the third factor, that is to cut down the parasitic capacitances. This can be done by employing the shorter channel lengths, smaller device dimensions and linewidths, in other words, the tighter mask tolerances.

The preceding discussion has assumed a given integration density. However, the integration density has been rapidly increasing year by year. So, the next question is what will happen with the increase of the de-

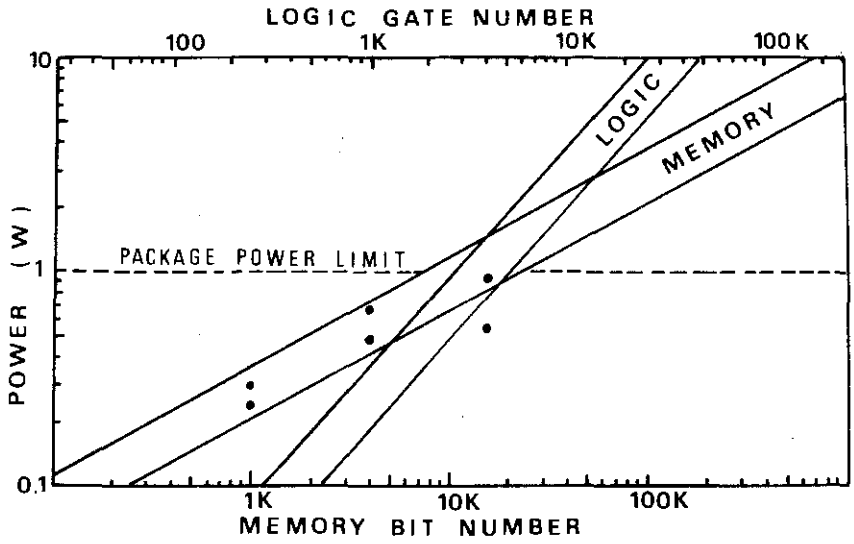


Figure 2.1 Relationship between integration scale and power in integrated circuits. Dots represent some of the actual data in memories.

vice number integrated on a chip, if the factors in the preceding paragraphs are kept unchanged. Figure 2.1 illustrates the general tendency of the power increase in logic and memory integrated circuits. The horizontal scale is the bit number in memory circuits and the gate number in logic circuits. The curves are drawn for n- and p-channel devices, and the CMOS devices are excluded. Some actual points are shown as dots for 1 K to 16 K memory circuits in the figure. Since the total power in logic circuits is determined by the number of the load transistors that accompany the gates, the power is in proportion to the gate number. In memory circuits, the power is mainly consumed by the peripheral circuits, such as input and output buffers, addressing circuits, sense amplifiers and timing pulse generators. This is because the memory cells are operated in a dynamic mode and thus consume relatively small power. Since the number of the peripheral circuits increases in proportion to $(\text{bit number})^{\frac{1}{2}}$, the corresponding power increase is in proportion to $(\text{bit number})^{\frac{1}{2}}$, too. However, a certain limitation exists in the number of the cells attached to a data line due to the increase of the data line capacitance. Due to the fact that the sense amplifiers are shared by the memory cells one can not refresh all the cells at a time. The time needed for refreshing all the cells is given by (cycle time) x (number of the word line), and the refresh period should be less than some fraction of the total time. This discussion suggests that in a very large scale memory, the power might increase in proportion to (bit number), because of the necessity to increase the number of the data line.

It should be noted that in actual situation, the circuit and device innovations, and clever designs push down the power vs. integration density curve year by year. This has resulted in a less steep line than the expectation shown in Fig. 2.1. It should, however, be pointed out that the most recent development of 16 Kbit memories [1], [2] or 16 bit microprocessors [3] indicates

that these circuits already consume almost the maximum power allowed for existing packages. Therefore, attacks to solve the power problems are the most important subject to develop more advanced integrated circuits and systems.

2.2 Power Comparisons for MOS Circuits

The basic cell for digital circuit is an inverter. There are essentially four types of cells that are frequently used in integrated circuits. These are:

(1) Enhancement load (Enhancement/Enhancement, E/E) static inverter.
(2) Depletion load (Enhancement/Depletion, E/D) static inverter.
(3) Complementary MOS (CMOS) static inverter.
(4) Multi-phase dynamic inverter.

Figure 2.2 illustrates these inverter circuits and the simplified circuits to explain the operation. By using these schematics, the power, delay and the power-delay product are calculated. The results are summarized in Table 2.1.

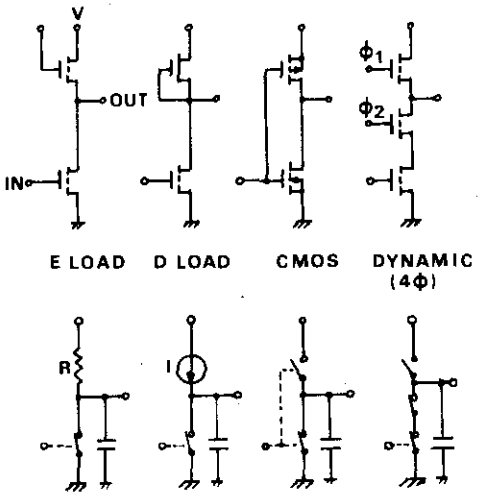


Figure 2.2 Basic inverter circuits for power comparison.

Table 2.1 First order approximation of power, delay and power-delay product for MOS inverters. The power loss in CMOS and dynamic circuit occurs at the switching transistors.

	E-LOAD	D-LOAD	C MOS & DYNAMIC
POWER P	$\frac{1}{2}\frac{V^2}{R}$	$\frac{1}{2}IV$	CV^2f
DELAY t_d	RC	$\frac{1}{2}\frac{CV}{I}$	$r_{on}C$
P x t_d	$\frac{1}{2}CV^2$	$\frac{1}{4}CV^2$	$\frac{1}{2}r_{on}C^2V^2f$

The calculation in Table 2.1 is very simplified. For example, the delay time for the enhancement-load and the CMOS is simply expressed by the time constants. In CMOS, r_{ON} represents an equivalent value of the resistance when one of the transistors is "ON". Thus, r_{ON} represents the equivalent resistance of the n-channel device when the output node voltage goes from high to low, and it is for the p-channel device when the output node voltage goes from low to high. Also the depletion load is expressed as a constant-current source that is not exactly the case as will be described in Chapter 4. The delay time for the depletion-load is the time for the current source to charge up the output node capacitance to half of the supply voltage.

It should be noted that the power-delay products are in proportion to (capacitance at the output node)$^{1 \text{ to } 2}$, and (supply voltage)^2, for any of these circuits. This indicates that both the reduction of the capacitance and the supply voltage will reduce the power dissipation in any MOS circuits.

Another point to be noted in Table 2.1 is that the power increases with the increase of the operating frequency in CMOS and the dynamic circuits, whereas it is constant in static enhancement-load and depletion-load circuits. Figure 2.3 illustrates a brief comparison of the power vs. operating frequency curves for these circuits. In the figure, the comparison is made by assuming the same output node capacitances. Thus, the comparison is slightly advantageous for CMOS, in that r_{ON} for the p-channel device is usually larger than that of the n-channel device and the capacitance at the output node is larger than

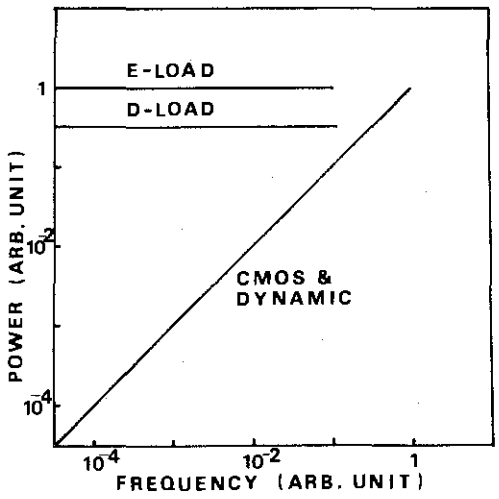


Figure 2.3 Power vs. operating frequency in various MOS integrated circuits.

that of other devices. The enhancement-load and the depletion-load are compared assuming the same delay time. If the same on-level, for instance $V_{ON} = 0.1\ V_{DD}$, is assumed, the calculated delay times are,

$t_d = 11\ r_{ON}C$ for enhancement-load

$t_d = 5\ r_{ON}C$ for depletion-load

Thus, the maximum frequency for the depletion-load inverter is twice as that of the enhancement-load inverter. In this case, since the power-delay product for the depletion-load inverter is half as that of the enhancement-load inverter, the corresponding power is almost the same.

In Fig. 2.3, although the power for the enhancement-load and the depletion-load inverters stays constant, it is possible to alter the ratio of the driver and the load transistors so that the corresponding power is small for low speed applications. However, for such a design, it is necessary to have a load transistor with very long channel length because the width of the transistor is basically limited by the photolithography. Thus, this approach is impractical to achieve low power. The conclusion derived from this is that at low frequency, the CMOS and the dynamic circuit give the lowest power. It should be noted that the dynamic circuit can only be operated above a certain frequency f_{min}, that is determined by the junction leakage and the sub-threshold characteristics of MOSFET. Thus, CMOS will give the lowest power below the minimum frequency for the dynamic circuit.

The preceding discussions are done assuming the same supply voltage for all of the circuits. In actual cases, the enhancement-load and the dynamic circuit need higher supply voltages than those needed for the depletion-load and the CMOS. This is because the voltage loss occurs when the enhancement-type load or precharge transistor charges the capacitance at the output node. Typically, the enhancement-load and the dynamic circuit need supply voltages of more than 10 volts. The depletion-load circuit can be operated with a supply voltage of less than five

volts, and it is widely used at five volts because this is the same supply voltage as bipolar TTL logic circuits. The CMOS can be operated with a supply as low as 1.3 volts. This difference arises from the different shapes of the dc-transfer curves that correspond to the different values of the noise margins for each circuit. The typical design will show that the necessary supply voltages for the enhancement-load and the dynamic circuit is $5V_T$, $3V_T$ for the deplation-load, and $2V_T$ for the CMOS. It is seen, therefore, that to reduce the power for a specific circuit, the decrease of the supply voltage, e.g., the decrease of the threshold voltage is effective. There are a number of ways to control the threshold voltage in the present-day MOS technologies. The next Section will give a brief review for this.

2.3 Threshold Voltage Control in the MOSFET

Sah and Pao [4] have given the threshold voltage equation that is widely used for standard type MOSFET. This is given by,

$$V_T = \phi_{MS} + 2\phi_F - \frac{qN_{ss}}{C_{OX}} + \frac{(2q\epsilon_s N)^{1/2}}{C_{OX}} (2\phi_F + V_{BB})^{\frac{1}{2}}. \qquad (2.1)$$

The equation illustrates that the techniques for the threshold voltage control as lined-up below are applicable.

(1) The choice of the gate metals or semiconductors. (ϕ_{MS})
(2) The substrate doping. (N)
(3) The substrate bias. (V_{BB})
(4) The oxide thickness. (C_{OX})
(5) The choice of (100) or (111) crystal orientation. (N_{ss})

Some other methods that are not illustrated by the Equation (2.1) are:

(6) Ion-implantation into the channel region.
(7) Addition of another insulator over SiO_2, such as Al_2O_3.

These are the methods that add a new term $\Delta V_T = qN_{ADD}/C_{OX}$ to the Eq. (2.1). Figure 2.4 illustrates some of the threshold control methods that are currently being used in mainly n-channel integrated circuits.

It should be pointed out that the threshold control exhibits somewhat different aspects in the case of p-channel devices. As can be seen in Fig. 2.5, the normal threshold voltage for the p-channel device is negative, that is, the p-channel device is an enhancement-mode. Thus, the main effort is on making low threshold and depletion mode devices. In n-channel devices, however, if one fabricates a transistor having a typical gate oxide thickness of 1000 Å, and a substrate doping density of 10^{15} cm^{-3}, the threshold voltage is slightly negative. The main effort is, therefore, on making enhancement mode devices because this is required to construct directly-coupled digital circuits. Various methods shown in Fig. 2.4 are now being widely used by a number of manufacturers in order to obtain a desired shift illustrated in Fig. 2.5. In the n-channel devices, the threshold shift to have a depletion mode device is also extensively used.

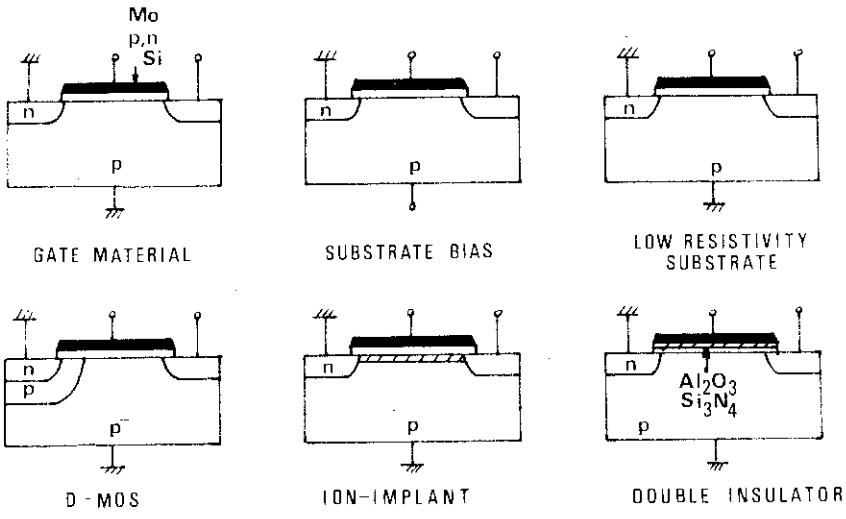


Figure 2.4 Threshold control techniques used for n-channel MOSFETs.

Various problems associated with these threshold control techniques are illustrated in Fig. 2.5. First, in standard MOSFET, that does not have any doping gradient in the channel region, the behavior of the current near and below the threshold voltage has become important. This arises from the necessity to lower the threshold voltage. A device design taking the subthreshold region over a wide range of substrate doping and oxide thickness has become inevitable in the design of low-voltage integrated circuits. Second, due to the necessity to control the threshold voltage over a wide range both positively and negatively, the use of ion-implantation has become advantageous. This introduces a non-uniform doping toward the direction perpendicular to the surface. The resulting current behavior is different from that of the standard MOSFET. For instance, the subthreshold tail current in the n-channel enhancement mode device, and the residual current in the p-channel and n-channel depletion mode devices are influenced by the ion-implantation significantly. Finally, there are a number of attacks to get a higher transconductance in a given transistor geometry to achieve a higher switching speed. The double-diffused MOS transistor is one of the technologies for this. Since the double-diffused MOSFET has a gradient of doping along the channel, the current does not obey the equations used for the standard MOSFET.

These problems associated with the threshold shift will be studied in Chapter 3 in detail.

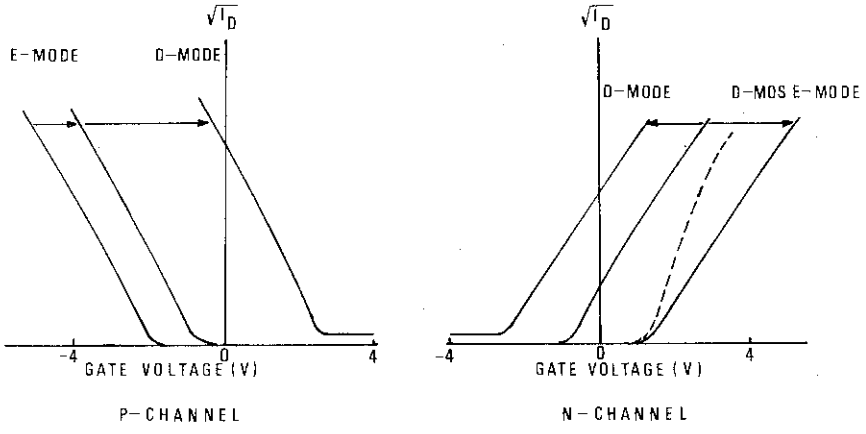


Figure 2.5 Threshold shifts in p and n-channel MOSFETs.

CHAPTER 3 MOSFET MODELS AND ANALYSES FOR LOW VOLTAGE APPLICATIONS

3.1 Introduction

Recent advances in MOS processing technology have made possible several types of MOS transistors utilized in actual circuits. These are:

(1) Standard p- and n-channel MOSFETs having a uniformly doped substrate.

(2) Ion-implanted MOSFETs with non-uniform doping of impurity toward the direction perpendicular to the surface.

(3) Double-diffused MOSFETs having non-uniform doping along the source-to-drain direction.

Various models and analyses with varying degree of approximation have been developed for these MOSFETs. Some of them aim understanding the physical behavior, some give practical expression for the drain current that is suitable for circuit analysis and design. Also, a number of numerical analyses for these transistors have been published.

In this chapter, the dc-current behavior of these transistors are studied in detail. First, in Section 3.2, existing theories and analyses of MOSFET current behavior are reviewed. Then, in Section 3.3. a new model of standard MOSFET that is capable of handling the drain current both in normal operation region and subthreshold region, will be proposed. The background for this is that the subthreshold current has become of special importance in the recent design of low-voltage circuits. Section 3.4 describes a numerical analysis of the subthreshold current in ion-implanted MOSFETs. Optimum implantation conditions for controlling both the threshold voltage and the subthreshold current are studied for single and double implanted cases. The double-layer implantation is proposed to obtain an independent control

of the threshold voltage and the subthreshold current. The last section (3.5) deals with the double-diffused MOSFETs. This technology assumes an increasing importance in low power circuit because of its small power-delay product due to effectively short channel length. A numerical analysis is given from the viewpoint of providing a physical understanding of the device operation and to give a good prediction of the current, internal potential and field distributions in various types of double-diffused MOSFET structure.

3.2 Several Existing Theories on dc-Behavior of MOSFET

A brief review of the existing theories on MOSFET dc-current is presented in this section.

The simplest model of Hofstein [1] has been widely used for practical purposes such as circuit analysis where the fast computation time is the important factor. The model uses so-called gradual channel approximation in that the field toward the source to drain direction is assumed to be relatively small in comparison to the surface field. The model neglects the effect of the bulk charge upon the current-voltage relationship, but it is included in the threshold voltage equation. The current expressions for this model are:

(1) Cutoff region $V_G - V_S \leq V_T$

$$I_D = 0 \tag{3.1}$$

(2) Saturation region $0 < V_G - V_S - V_T < V_D - V_S$

$$I_D = (\beta/2)(V_G - V_S - V_T)^2 \tag{3.2}$$

(3) Nonsaturation region $V_D - V_S \leq V_G - V_S - V_T$

$$I_D = \beta\left[(V_G - V_S - V_T)(V_D - V_S) - \tfrac{1}{2}(V_D - V_S)^2\right], \tag{3.3}$$

in which V_S, V_G and V_D are source, gate and drain voltages with respect to the substrate, and β is a conductance constant given by

$$\beta = \frac{W \epsilon_{OX}}{L T_{OX}} \mu \ . \qquad (3.4)$$

Some of the general-purpose circuit analysis programs are using the modified expressions of this model. One of the examples is Schichman-Hodges model [2] used in the circuit analysis program SPICE [3].

Some of the drawbacks that arise from its too simple approximation are:

(1) The expressions are not accurate near and above the pinch-off voltage where the bulk charge in the surface depletion region affects the saturation drain voltage.

(2) Mobility is actually a function of the surface and the drain field.

(3) The channel length modulation effect is not included in the model.

(4) The equations are not valid below and just above the threshold voltage where the diffusion current can not be neglected.

Further studies thus have led to more accurate and more sophisticated models taking account of these. Let us discuss some of the important modifications that are added to the simple model.

(A) Bulk Charge Effect

The effect of bulk charge has been introduced by Ihantola and Moll [4], and Sah [5]. In their models, the charge in the surface depletion layer was considered to be a function of the position corresponding to the variation of the surface potential. This gives rise to a lower saturation drain voltage than that expected by the simple Hofstein model. The equations for the drain current in this case are as follows.

(1) Cut-off region: $V_G < V_T$

$$I_D = 0 \tag{3.5}$$

(2) Saturation region: $V_G \geq V_T$, $V_D \geq V_{DS}$

$$I_D = \frac{W}{L} \mu C_{OX} \left\{ \left[V_G - V_{FB} - 2\phi_F - \frac{V_{DS}}{2} \right] V_{DS} - \frac{2\sqrt{2q\epsilon_s N_A}}{3 C_{OX}} \left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2} \right] \right\} \tag{3.6}$$

(3) Non-saturation region: $V_G \geq V_T$, $V_D < V_{DS}$

$$I_D = \frac{W}{L} \mu C_{OX} \left\{ \left[V_G - V_{FB} - 2\phi_F - \frac{V_D}{2} \right] V_D - \frac{2\sqrt{2q\epsilon_s N_A}}{3 C_{OX}} \left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2} \right] \right\}, \tag{3.7}$$

where V_{DS} is the saturation drain voltage given by the equation,

$$V_{DS} = V_G - V_{FB} - 2\phi_F + \frac{\epsilon_s q N_A}{C_{OX}} \left[1 - \left(1 + \frac{2 C_{OX}^2 (V_G - V_{FB})}{\epsilon_S q N_A} \right)^{1/2} \right]. \tag{3.8}$$

This model is a good approximation when the gate voltage is well above the threshold voltage and when the channel length is large. For this reason, the model has been used as a basis of the current equations in some of the circuit analysis programs together with some other minor modifications such as the finite drain conductance in the saturation region, mobility decrease due to the gate field and the dynamic change of the gate-source and the gate-drain capacitances. Benchkowsky model [6] is one of the examples that this model is utilized for practical purposes. It should, however, be noted that the model is again not applicable in the low current region near the threshold voltage, where the assumption that the surface potential at the source is pinned to $2\phi_F$, is not accurate. The model should be modified in this current range.

(B) Finite Drain Conductance in the Saturation Region

In the preceding models, the current in the saturation region does not vary with the increase of the drain voltage. However, in actual cases, finite drain conductance is observed. This is caused by the drain field that attracts the channel carriers toward the drain. Thus gradual channel approximation does not hold when the drain field is higher than the gate field. Consequently, the effective channel length is somewhat shorter than the actual source-to-drain spacing. The simplest theory to explain this phenomenon was proposed by Reddi and Sah [7]. In their report, the effective channel length was given by substracting the depletion layer width from the source-to-drain spacing, where the depletion layer width is approximated by the plane junction theory as seen by the equation,

$$L_{eff} = L - \left[\frac{2\epsilon_s}{qN_A} (V_D - V_{DS}) \right]^{1/2} . \qquad (3.9)$$

However, the experimental results indicates much larger drain conductance as compared to the equation (3.9). The descrepancy is caused by the two-dimensional nature of MOSFET operation, that is, the drain depletion layer is under the influence of the gate field, and the thickness of the oxide and the depth of the drain diffusion affect the field in the drain depletion region. To take account of these factors, two dimensional analysis is inevitable. It has been shown by Schroeder and Muller [8], that the two dimensional approach gives a good agreement of the calculated and measured currents in the saturation region. Since this effect is substantially important in short channel devices, a number of numerical analysis programs with varying degree of approximations have appeared recently, for instance those of Kennedy [9], Hachitel [10], Vandorpe [11], Mock [12].

An analytical approach to evaluate the channel shortening

effect more accurately than Eq.(3.9), was proposed by Bentchkowsky [13]. The two dimensional nature was introduced by the semi-empirical form as seen by the equation,

$$\frac{dl_{dep}}{dV_D} = \frac{\epsilon_S T_{OX}}{\epsilon_{OX}} \frac{(\beta - \alpha)(V_G' - V_{DS})}{[\alpha(V_D - V_G') + \beta(V_G' - V_{DS})]^2} \tag{3.10}$$

$$I_D = \frac{I_{DS}}{L\,(1 - l_{dep}/L)^2}, \tag{3.11}$$

where $V_G' = V_G + Q_{ss}/C_{OX}$ and α and β are constants having values $\alpha = 0.2$ and $\beta = 0.6$. These parameters are determined so that a good fitting of the current in the saturation region to the measurements would be obtained.

In this thesis, the models and analyses that will be discussed in Section 3.3 and 3.4, and the design of enhancement-depletion circuits in Chapter 4 do not take into account the channel shortening effect. Thus, to apply the results of these to MOS transistors having short channel lengths, a modification of the theory is needed. This can be handled by using Eq. (3.10) and Eq. (3.11) together with the results obtained in these Chapters.

(C) Mobility Variations due to Gate and Drain Field

It is well known that mobility of the carriers in the surface channel is a function of the surface field E_x, source-to-drain field E_y and impurity doping density N. Crystal orientation, surface state density and the temperature also affect the mobility significantly. It is seen, therefore, that this is one of the most complex problems in modelling the MOS transistors. As far as the author knows, there have been so far no satisfactory theory that is capable of handling all of these effects.

There are, however, a number of reports that give explanations both theoretically and experimentally to the mobility variation due to various parameters stated previously.

The gate field dependence of mobility has been extensively studied by a number of theorists; Schrieffer [14], Greene [15], Sah, Ning and Tschopp [16], and Pierret and Sah [17]. Also, several papers have been published on experimental studies of the gate field dependence of mobility. [18], [19] The agreement between the theories and the experiments is, however, not satisfactory.

For practical purposes, a semi-empirical form that is developed by Crawford [20], is often used. This utilizes a constant θ_a having a dimension of $(\text{volt})^{-1}$ as seen by the equation,

$$\mu = \mu_0 \frac{1}{1 + \theta_a (V_G - V_T)} \quad . \tag{3.12}$$

Bentchkowsky have developed another form of mobility that utilizes an average surface field E_s as seen by the equation,

$$\mu = \mu_0 \left(\frac{E_{s0}}{E_s} \right)^{c_1} , \tag{3.13}$$

where E_{s0} and c_1 are constants having values $c_1 = 0.36$ for electrons and $E_{s0} = 6 \times 10^4$ V/m. [21]

The drain field dependence of mobility in the surface channel and drain depletion region is not well understood because of the difficulty to apply a high uniform field for measurements. This is because the field in MOS transistors is basically non-uniform when it is biased to a high drain voltage. Some experimental results [22], [23] indicate that the velocity-field relationship of electrons and holes in the surface channel is similar to the form in bulk. However, accurate form of mobility near the saturation velocity under the influence of the gate field is not obtained. Taking account of these, the present status is that

the form of mobility dependence on field used in the bulk is often employed in analysing MOS transistors having short channel lengths where the effect of velocity saturation is an important factor. One example for this is given by the form,

$$\mu = \mu_0 \left[1 + \left(\frac{E_y}{E_c} \right) \right]^{-1/\alpha} , \qquad (3.14)$$

where $\alpha = 1$ for holes and $\alpha = 2$ for electrons. [24]

Throughout this thesis, the gate field dependence given by Eq.(3.12) and a modified form is used. The modified form expresses the mobility as a function of the gate field, not of the gate voltage, by using a constant θ (m/V). Equation (3.14) will be used to analyse double-diffused MOSFETs in which local electric field concentration plays an important role.

(D) A Numerical Analysis of MOSFET Incorporating Diffusion Component in the Current Expression

The preceding theories of Hofstein or Ihantola and Moll did not include the diffusion component in the current expressions. Pao and Sah [25] have performed a one-dimensional numerical integration of the current equation that is given by the form,

$$I_D = \frac{W}{L} \int_0^L \mu \left(\frac{kT}{q} \right) q N(y) \frac{d\xi}{dy} \, dy , \qquad (3.15)$$

where ξ is quasi-Fermi potential measured from bulk Fermi potential, $N(y)$ is induced electron number at the surface. Thus, the drain current is basically the sum of the drift and the diffusion components. The induced electron number is approximated by using the gradual channel approximation. This is again given by the numerical integration as seen by the equation,

$$N(y) = N_I L_{DI}$$

$$\int_{U_F}^{U_{SF}} \frac{\exp(U - \xi - U_F)\, dU}{[\exp(U_F - U) - \exp(U_F) + \exp(U - \xi - U_F) - \exp(-\xi - U_F) - U\exp(-U_F) + U\exp(U_F)]^{1/2}}, \tag{3.16}$$

In order to calculate the current, one has to integrate Eqs. (3.15) and (3.16) numerically. These steps need considerable computation time, and this limits the applicability of the model. Two dimensional analysis provides better accuracy than this model does with basically the same computer time. It is, however, noted that these equations are valid in analysing the subthreshold currents of MOS transistors in that the diffusion current is dominant. For this reason, several models on subthreshold current behavior have been developed based on this analysis. In Section 3.3, a new set of equations that states the MOSFET current behavior in the entire operating region, will be proposed. This new model is based on these equations.

There are a number of phenomena in the dc-behavior of MOS transistors that can not be analysed by one-dimensional equations because of the two dimensional nature of the transistor operation. Specifically, the recent advances of photolithography have made it possible to fabricate MOSFETs having very small dimensions. This has led to the necessity to investigate various two dimensional effects such as; (1) the threshold voltage decrease with the decrease of the channel length, (2) the dependence of the threshold voltage on the drain voltage and the substrate bias, (3) the punch-through current and the increase of the drain conductance in the saturation region, (4) the substrate current, (5) the decrease of the breakdown voltage due to the high field and parasitic bipolar transistor, etc..

In order to study these phenomena, two-dimensional analysis programs with varying degree of approximation have been developed

as stated previously. From a practical point of view, the computer time needed is still too long. For some purposes that need a lot of calculations, the use of two-dimensional programs is costly. One of the examples of this is the optimization of the device structures that needs the calculation of the current voltage relationships with various variables as parameters such as channel lengths, oxide thicknesses and ion-implantation conditions. It is, however, a very powerful tool for some limited purposes; (1) the calculation of device parameters including two-dimensional effects for the model used in circuit analysis, (2) prediction of the device behavior in a new device structure without fabricating the device.

Since a lot of effort is consumed on the development of MOS integrated circuits utilizing shrunk MOS transistors, the importance of the two-dimensional analysis will certain to increase. It appears that the progress of both numerical analysis techniques and the computer itself will make this approach more versatile.

3.3 A MOSFET Model Including Subthreshold Region [30], [31], [32]

3.3.1 Introduction

It has been pointed out in Chapter 2 that the reduction of the operating voltage and the use of the dynamic or the CMOS circuits are the most successful solutions to reduce power. However, very small currents of less than a microampere give rise to a limit for low voltage operation of the circuits. This limitation is especially important in the dynamic circuits. The low level current in standard MOSFET biased below the threshold voltage is called "subthreshold current" or "tail current". The latter comes from its characteristic feature in $(I_D)^{\frac{1}{2}} - V_G$ curve. Therefore, a precise circuit design incorporating the tail current is inevitable for integrated circuits with low supply voltage, e.g., low threshold voltage. Taking the dynamic memory circuit as an example, even an operation of five to ten volts requires a careful determination of the substrate doping and oxide thickness. This is because the threshold voltage, that is defined as the gate voltage when the surface potential is twice Fermi potential at the source end of the channel, of around one volt is necessary, and even if the gate swing is several hundred millivolts below the threshold voltage, a weakly inverted channel can cause a leak current path. Consequently, memory characteristics are deteriorated, resulting in a too short storage time.

Several classical MOSFET models that are described in Section 3.2 are not appropriate for the purpose stated previously. Hayashi and Tarui [26], Barron [27], and Troutman [28], have proposed equations that are applicable to the tail current region. Swanson and Meindl [29], have proposed a set of equations covering the entire operating region of MOSFET, in that the weak inversion region and the strong inversion region is connected so that the slope of the current vs. gate voltage curves is continuous. This

was done by introducing an additional parameter ϕ which shifts the current-voltage relationship in the strong inversion region.

In this section, a new set of analytical expressions of the drain current is described. These are obtained from the integral form of the drain current given by Pao and Sah. [25] One of the key features of the model is that several characteristic surface potentials are used as the explicit parameters in the current expressions under both the strong and the weak inversion conditions. An advantage of using the surface potentials is that the connection of the current solutions in the tail current and the saturation regions becomes continuous without introducing additional fitting parameters.

An extensive comparison of the theoretical and experimental I_D vs. V_D and I_D vs. V_G curves for fabricated n-channel devices will be made. The dependence of these characteristics upon substrate doping density, oxide thickness and temperature will be studied both experimantally and theoretically. Application of the model to actual circuit designs will be described taking a dynamic memory and a low voltage static inverter circuit as examples.

3.3.2 Drain Current Expression

The integral form of the drain current given by Pao and Sah is

$$I_D = \frac{W}{L} \int_0^L \mu \left(\frac{kT}{q}\right) q \left(\frac{d\xi}{dy}\right) N(y)\, dy, \qquad (3.17)$$

where L and W are the channel length and width, and μ is effective mobility. N (y) is the total induced electron number that is given by the integration (3.16) in Section 3.2. Gate voltage U_G is related to the surface potential U_{SF} as seen by the equation,

$$U_G \simeq U_{SF} + \gamma[\exp (U_{SF} - \xi - U_F) + (U_{SF} - 1) \exp (U_F)]^{1/2}, \qquad (3.18)$$

where the potentials denoted by U are in the unit of (kT/q). In the preceding equation, U_G is an effective gate voltage. In other words, the effect of the work function difference ϕ_{ms}, and the fixed charge in the insulator N_{ss} are not included. γ is the ratio C_D/C_{OX} where C_D is Debye capacitance that is given by the equation,

$$C_D = \frac{\epsilon_S}{L_{DI}} . \tag{3.19}$$

Although the numerical calculation of Eq. (3.17) and Eq. (3.18) gives the drain current including both the drift and the diffusion terms, it is desirable that the drain current be explicitly expressed as functions of the drain voltage, the gate voltage and the source voltage for practical purposes.

The approach taken in this section is that the charge equations are approximated separately according to the strong or the weak inversion conditions of the channel, and the special values of the surface potentials are used to get an accurate approximation in both regions.

In this model, three operation regions of MOSFET as illustrated in Fig. 3.1 are considered seperately. This makes clear the potential variation in each region. First, in the tail current region, the surface potential is almost constant throughout the channel, and quasi-Fermi potential only varies. This means that

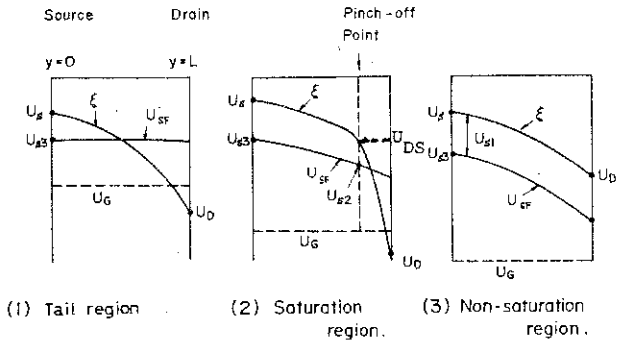


Figure 3.1 Illustration of the shape of U_{SF} and ξ in three operation regions of MOSFET.

the diffusion component dominates throughout the channel. Second, in the nonsaturation region, strongly inverted surface is formed throughout the channel. The drift component is dominant in this region, and quasi-Fermi potential is almost in parallel relationship with the surface potential. Finally, in the saturation region, the drift component is dominant in the source side of the channel. However, in the region close to the drain, the gate field is not strong enough to sustain the channel. It is assumed that at the point where quasi-Fermi potential is equal to the saturation drain voltage U_{DS}, pinch-off occurs. The channel beyond the pinch-off point is assumed to be weakly inverted. It should be pointed out these approximations are totally one-dimensional. Thus, the effect of the strong drain field near the drain diffusion is not taken into account. When the drain field is large enough, the channel charge is injected from the channel into deeper part of the body and travels toward the drain. This is so called channel shortening condition. Therefore, for short channel devices, the model should be modified incorporating this effect by using Eqs. (3.10) and (3.11) in Section 3.2.

In order to obtain accurate current expressions, the surface potentials U_{S1}, U_{S2}, U_{S3} as shown in Fig. 3.1 are used. These are given by solving the equations,

$$U_G \simeq U_{S3} + \gamma[\exp(U_{S3} - U_S - U_F) + (U_{S3} - 1)\exp(U_F)]^{1/2} \tag{3.20}$$

$$U_{S1} = U_{S3} - U_S \tag{3.21}$$

$$U_G \simeq U_{S2} + \gamma[\exp(U_{S2} - U_{DS} - U_F) + (U_{S2} - 1)\exp(U_F)]^{1/2}. \tag{3.22}$$

Here, U_S is the source voltage, and U_{DS} is the saturation drain voltage given by Eq. (3.33).

One of the features of the present model is that the classical concept of the threshold voltage, the voltage at which the

drain current starts to flow, can not be applied. In the classical theories, the threshold has usually been defined by the gate voltage when the surface potential U_{S1} at the source is equal to twice Fermi-potential as seen by the equation,

$$U_T = 2U_F + \gamma(2U_F + U_S)^{1/2} \exp(U_F/2) + U_S. \tag{3.23}$$

This equation assumes that the surface potential U_{S1} is pinned when the inversion layer exists. However, Eqs. (3.20) and (3.21) indicates that U_{S1} actually increases gradually with the increase of the gate voltage in the strong inversion region. Consequently significant error is observed near the threshold voltage in the classical models. For instance, the given threshold does not coincide with the extended threshold from $(I_D)^{\frac{1}{2}} - V_G$ or $g_D - V_G$ curves as will be demonstrated experimentally. In the present theory, U_{S1} is a varying parameter both in the weak and the strong inversion region.

Electron charge Q_N is approximated as follows. Total charge Q_{SF} that is the sum of the electron charge and the bulk charge is given by,

$$Q_{SF} = -C_O\left(\frac{kT}{q}\right)(U_G - U_{SF}) \tag{3.24A}$$

$$= -C_D\left(\frac{kT}{q}\right)[\exp(U_{SF} - \xi - U_F) + (U_{SF} - 1)\exp(U_F)]^{1/2}. \tag{3.24B}$$

Thus the induced electron charge is given by,

$$Q_N = Q_{SF} - Q_B \tag{3.25}$$

where Q_B is the fixed bulk charge in the surface depletion layer. Detailed analysis of the bulk charge under the strong inversion condition was given by Sah and Pao [33] in that the bulk charge was obtained by dividing the charge distribution into three regions. It was shown that the major contribution comes from the

surface depletion region. In the present analysis, the bulk charge under both the strong and the weak inversion condition is approximated by

$$Q_B \simeq - C_D \left(\frac{kT}{q}\right) [(U_{SF} - 1) \exp [U_F]]^{1/2}. \tag{3.26}$$

If $U_{SF} = U_S + 2U_F$ is assumed, the preceding equation coincides with the simple bulk charge approximation taking only the contribution from the surface depletion region. Although the detailed three-region analysis gives more accurate result than Eq. (3.26), practically the approximation gives a sufficient accuracy.

For the strongly inverted surface, using (3.24A), Q_N is approximated by,

$$Q_N \simeq - C_O \left(\frac{kT}{q}\right) \{U_G - U_{SF} - \gamma[(U_{SF} - 1) \cdot \exp (U_F)]^{1/2}\}. \tag{3.27}$$

If the surface is weakly inverted, using (3.24B) and (3.26), Q_N is given by,

$$\begin{aligned} Q_N \simeq - C_D \left(\frac{kT}{q}\right) \{&[\exp (U_{SF} - \xi - U_F) \\ &+ (U_{SF} - 1) \exp (U_F)]^{1/2} - [(U_{SF} - 1) \\ &\cdot \exp (U_F)]^{1/2}\} \end{aligned} \tag{3.28A}$$

$$\simeq - C_D \left(\frac{kT}{q}\right) \frac{\exp (U_{SF} - \xi - 1.5U_F)}{2 (U_{SF} - 1)^{1/2}}. \tag{3.28B}$$

Next, let us calculate the drain current in each operation region illustrated in Fig. 3.1 by substituting the preceding approximation for Q_N into Eq. (3.17).

(1) Tail Current Region; $U_G \leq U_T$ (or $U_{S1} \leq 2U_F$)

In this region, Q_N is given by Eq. (3.28) throughout the entire channel. Since at the source and the drain junction, quasi-Fermi potential ξ is equal to the voltage applied to the junc-

tion, the drain current integral can be rewritten as an integral in the voltage domain as seen by the equation,

$$I_D \simeq \frac{W}{L}\mu\frac{C_D}{2}\left(\frac{kT}{q}\right)^2 \int_{U_S}^{U_D} \frac{\exp(U_{SF} - \xi - 1.5U_F)}{(U_{SF}-1)^{1/2}}\, d\xi. \tag{3.29}$$

It should be noted here that U_{SF} is nearly constant throughout the entire channel because the first term in $(\ )^{\frac{1}{2}}$ in Eq. (3.18) is small. Therefore, U_{SF} can be represented by U_{S3} in Eq. (3.20). Performing the integration, we have

$$I_D \simeq \frac{W}{L}\mu\frac{C_D}{2}\left(\frac{kT}{q}\right)^2 \frac{\exp(U_{S3} - 1.5U_F)}{(U_{S3}-1)^{1/2}} (\exp(-U_S) - \exp(-U_D)). \tag{3.30}$$

This expression is basically the same as the equations that have already been given by Hayashi and Tarui [26], and by Barron [27].

(2) Nonsaturation Region; $U_G > U_T$ (or $U_{S1} > 2U_F$) and $U_D \leq U_{DS}$

In this case Q_N is given by Eq. (3.27). The drain current integral in the voltage domain becomes,

$$I_D \simeq \frac{W}{L}\mu C_O\left(\frac{kT}{q}\right)^2 \int_{U_S}^{U_D} \{U_G - U_{SF} - \gamma[(U_{SF}-1)\exp(U_F)]^{1/2}\}\, d\xi. \tag{3.31}$$

It should be noted that quasi-Fermi potential ξ and the surface potential U_{SF} are almost in parallel relationship throughout the entire channel, that is to say $U_{SF} \simeq U_{S1} + \xi$. By practicing the integration, we obtain

$$I_D = \frac{W}{L}\mu\left(\frac{kT}{q}\right)^2 \{C_0[(U_G - U_{S1})(U_D - U_S) - \tfrac{1}{2}(U_D^2 - U_S^2)] - \tfrac{2}{3}C_D\exp(U_F/2) \cdot[(U_D + U_{S1} - 1)^{3/2} - (U_S + U_{S1} - 1)^{3/2}]\}. \tag{3.32}$$

The preceding equation coincides with the Reddi-Sah analysis

when $U_{S1} = 2U_F$. As has been discussed in the preceding paragraph, U_{S1} is left as a function of the gate voltage in the present theory. This means that the gate voltage-dependent threshold is equivalently introduced in the strong inversion condition. This results in a somewhat modified current vs. gate voltage relationship just above the threshold in comparison to the classical theories. For instance, $(I_D)^{\frac{1}{2}} - V_G$ curve in the saturation region is bent when the gate voltage is low, and it is smoothly connected to the tail current region.

(3) Saturation Region; $U_G > U_T$ (or $U_{S1} > 2U_F$) and $U_D > U_{DS}$

The pinch-off drain voltage is obtained from Eq. (3.32) by assuming $dI_D / dU_D = 0$. The result is

$$U_{DS} = -(U_{S1} - 1) + \tfrac{1}{4}\{2\gamma^2 \exp(U_F) + 4(U_G - 1) - 2\gamma \exp(U_F/2)[\gamma^2 \exp(U_F) + 4(U_G - 1)]^{1/2}\}. \quad (3.34)$$

When the drain bias is above the saturation drain voltage U_{DS}, the channel between the pinch-off point and the drain diffusion becomes weakly inverted or depleted, whereas the channel between the source diffusion and the pinch-off point stays strongly inverted. Thus, the integration (3.17) can be divided into two regions and seen as

$$I_D = \frac{W}{L}\mu\left(\frac{kT}{q}\right)\left[\int_{U_S}^{U_{DS}} Q(\xi)\, d\xi + \int_{U_{DS}}^{U_D} Q(\xi)\, d\xi\right]. \quad (3.35)$$

The first term is integrated in a similar manner as in Eq.(3.32). The second integration differs from Eq. (3.30) in that surface potential U_{S2} should be used instead of U_{S3}. This yields

$$I_D \simeq \frac{W}{L}\mu\left(\frac{kT}{q}\right)^2\left\{C_O[(U_G - U_{S1})(U_{DS} - U_S) - \tfrac{1}{2}(U_{DS}^2 - U_S^2)] - \tfrac{2}{3}C_D \exp(U_F/2)\right.$$
$$\cdot[(U_{DS} + U_{S1} - 1)^{3/2} - (U_S + U_{S1} - 1)^{3/2}] + \frac{C_D}{2}\frac{\exp(U_{S2} - 1.5U_F)}{(U_{S2} - 1)^{1/2}}$$
$$\left.\cdot[\exp(-U_{DS}) - \exp(-U_D)]\right\}. \qquad (3.35)$$

The drain current expressions described in the preceding paragraphs cover the entire operation region of MOSFET.

It is important to take into accout the temperature dependence and the gate voltage dependence of the surface electron mobility. The mobility equations employed in the present model are,

$$U_G \leq U_T, \quad \mu = \mu(T = 300\ \mathrm{K})(T/300)^{\alpha} \qquad (3.36)$$

$$U_G > U_T, \quad \mu = \mu(T = 300\ \mathrm{K}) \cdot (T/300)^{\alpha} \Big/ \left[1 + \frac{kT}{q}\theta_s(U_G - U_T)\right]. \qquad (3.37)$$

In Eqs. (3.36) and (3.37) it is assumed that the mobility along the channel is constant. This assumption is valid for the device having relatively long channel length except in the region very close to the drain. An analysis including drain-field dependent mobility indicates, as in Fig. 3.39, that the reduced mobility due to the drain field can not be ignored for the device having a short channel length. The figure also shows that the varying gate-field toward the source-to-drain direction does not affect the mobility significantly in long channel cases.

Early investigation on the temperature dependence of surface mobility [18], indicates α is -1.5 for electrons at T = 300 K. Recently, Sah et al. [16] have shown that the temperature dependence of mobility should be expressed by a calculation taking both scattering by surface oxide charges and surface phonons into account, wherein the former mechanism has a temperature dependence

of T, and the latter has a temperature dependence of T^{-2} at T less than 150 K. In the present calculation, $\alpha = -1.5$ is empirically chosen.

In order to calculate the current value using this model one has to calculate Eqs. (3.20) to (3.22) numerically to obtain necessary surface potentials. This can be done by, for instance, Newton iteration, and does not need too much computer time. Approximate solutions of these equations by making use of a polynomial expansion can also be used.

The effect of fast surface states N_{fs} is not included in the present theory. This yields some modification of the effective gate voltage depending on the gate bias resulting in a less steep log I_D - V_G curve in a certain gate voltage range. The effect can be easily implemented in the model by adding a single term describing the fast surface states in Eqs. (3.20) to (3.22). It will be shown that the assumption does not cause significant error for (100) n-channel MOSFETs.

The obtained equations are summarized in Table 3.1.

Table 3.1 Expressions of the drain current and the surface potentials in the present theory.

Tail Current Region $U_{S1} < 2U_F$	$I_D=\frac{W}{L}\mu\frac{C_D}{2}\left(\frac{kT}{q}\right)^2\frac{e^{U_{S3}-1.5U_F}}{(U_{S3}-1)^{1/2}}(e^{-U_S}-e^{-U_D})$ (1)
Nonsaturation Region $U_{S1} \geq 2U_F$ $U_D < U_{DS}$	$I_D=\frac{W}{L}\mu\left(\frac{kT}{q}\right)^2\{C_O[(U_G-U_{S1})(U_D-U_S)-\frac{1}{2}(U_D^2-U_S^2)]$ $-\frac{2}{3}C_De^{U_F/2}[(U_D+U_{S1}-1)^{3/2}-(U_S+U_{S1}-1)^{3/2}]\}$ (2)
Saturation Region $U_{S1} \geq 2U_F$ $U_D \geq U_{DS}$	$I_D=\frac{W}{L}\mu\left(\frac{kT}{q}\right)^2\{C_O[(U_G-U_{S1})(U_{DS}-U_S)-\frac{1}{2}(U_{DS}^2-U_S^2)]-\frac{2}{3}C_De^{U_F/2}$ $\cdot[(U_{DS}+U_{S1}-1)^{3/2}-(U_S+U_{S1}-1)^{3/2}]+\frac{C_D}{2}\frac{e^{U_{S1}-1.5U_F}}{(U_{S2}-1)^{1/2}}(e^{-U_{DS}}-e^{-U_D})\}$ (3)
$U_G=U_{S3}+\gamma[e^{U_{S3}-U_S-U_F}+(U_{S3}-1)e^{U_F}]^{1/2}$ (4) $\quad U_{S1}=U_{S3}-U_S$ (5) $U_G=U_{S2}+\gamma[e^{U_{S2}-U_{DS}-U_F}+(U_{S2}-1)e^{U_F}]^{1/2}$ (6) $\quad \gamma=C_D/C_O$ (7) For $U_G > U_T$ $\mu=\mu(T=300\ K)(T/300)^{\alpha}/[1+\frac{kT}{q}\theta(U_G-U_T)]$ (8)	

3.3.3 Comparison with Experiments

Comparison of the model with experiments has been carried out by using n-channel annular gate MOSFETs fabricated on (100) surfaces. The gate insulator is SiO_2, and both aluminum and silicon gates were used. The impurity concentrations and the oxide thicknesses for the samples were varied to observe the applicability of the model in a wide range of parameters. These values are summarized in Table 3.2. The values of the oxide thicknesses were measured by the capacitance method and the ellipsometry. Substrate impurity concentrations were determined by using Eq. (2.1), that is, from the variation of the threshold voltage due to substrate bias. This makes possible an accurate measurement of the effective impurity concentration at the surface to avoid possible error caused by the depletion of boron during oxidation process.

To compare the measured and the calculated currents, it is desirable that the values of mobility μ, θ_a and N_{ss} are determined by some other methods precedingly. For this purpose, one has to measure the current-voltage curves at low drain voltage, and at the same time the corresponding surface potentials. It is, however, very difficult to measure the surface potential independently and accurately. For this reason, these parameters were determined by comparing the measured and the calculated points from the model by using a computer. This was performed in the following manner. First, approximate values of β_o, and N_{ss} were obtained from the simple Hofstein model using three points in the saturation region where the $(I_D)^{\frac{1}{2}} - V_G$ curve exhibits almost linear characteristics. Then, the value of θ_a was determined using other three points in the saturation region at higher gate voltages where $(I_D)^{\frac{1}{2}}$-V_G curve has smaller slope than the low gate voltage case. These values were adjusted by fitting the calculated currents from the present theory to the measured currents. At this stage, one point

Table 3.2 Samples used to compare the model to the experiments; The samples are n-channel annular gate MOSFETs fabricated on (100) surface.

Samples	Resistivity of the substrate (ohm.cm)	Impurity concentration (cm^{-3})	Oxide thickness (Å)	Gate
A-30	180 - 200	7×10^{13}	675	Al
B-30	180 - 200	7×10^{13}	1470	Al
C-30	180 - 200	7×10^{13}	5030	Al
A-50	17 - 30	7×10^{14}	675	Al
B-50	17 - 30	7×10^{14}	1470	Al
C-50	17 - 30	7×10^{14}	5030	Al
A-40	2 - 3	4×10^{15}	675	Al
B-40	2 - 3	4×10^{15}	1470	Al
C-40	2 - 3	4×10^{15}	5030	Al
S-1	8 - 12	1×10^{15}	1090	Si
S-3	8 - 12	1×10^{15}	600	Si
S-4	8 - 12	1×10^{15}	400	Si
S-5	8 - 12	1×10^{15}	220	Si

Table 3.3 Values of β_o, θ_a and N_{ss} for the samples.

Samples	Channel Conductance β_0 ($\mu\mho$/V)	Gate Voltage Dependence of μ $\theta_a(V^{-1})$	Fixed Charge in the Insulator N_{ss} ($\times 10^{11} cm^{-2}$)
A-30	1133.8	0.108	0.55
B-30	670.3	0.093	0.62
C-30	202.2	0.038	0.38
A-50	1185.0	0.110	0.59
B-50	628.0	0.080	0.64
C-50	181.0	0.034	0.65
A-40	1049.3	0.103	0.70
B-40	539.1	0.066	1.14
C-40	163.7	0.029	0.79

in the tail current region was added in order to get an accurate value of N_{ss} because I_D vs. V_G curve is shifted along V_G axis by varying N_{ss}. Consequently, seven points were used in the fitting procedure. Although the points in the saturation region were mainly used in the procedure, it was found that the model agrees well with the measurements in the entire region as will be shown in the succeeding paragraphs. Therefore, it appears that the values obtained are the good estimation for these parameters. Table 3.3 shows the values of β_0, θ_a and N_{ss} for Al gate samples.

Figures 3.2 -3.5 show the comparison of the measured and calculated log I_D - V_G characteristics. The dashed curve in Fig. 3.2 illustrates the calculated results from the classical models excluding the tail current. From these figures, it is seen that the theoretical curves are continuous and that the agreement with experiments is quite good over a wide range of gate oxide thickness and substrate doping density.

Figure 3.6 illustrates the temperature dependence of the log I_D - V_G curves. In the calculation, temperature dependences of Fermi potential U_F and mobility μ are taken into account. N_{ss}, T_{OX} and θ are assumed to be constant within this tamperature range, and the values obtained at 300 K are used. In the figure, the deviation below 10^{-10} A at relatively high temperature is observed. This is due to the recombination-generation current in the depletion layer both at the surface and at the junction. Additional current sources should be added in the present model in order to express the leakage currents. Another deviation occurs at the current level between 10^{-7} A and 10^{-4} A. This is due to either; incorrect approximation of the mobility within this range, error in estimating the surface potential, or the effect of the fast surface states. It is seen, for practical purposes, the present theory gives a good prediction of the current within this temperature range.

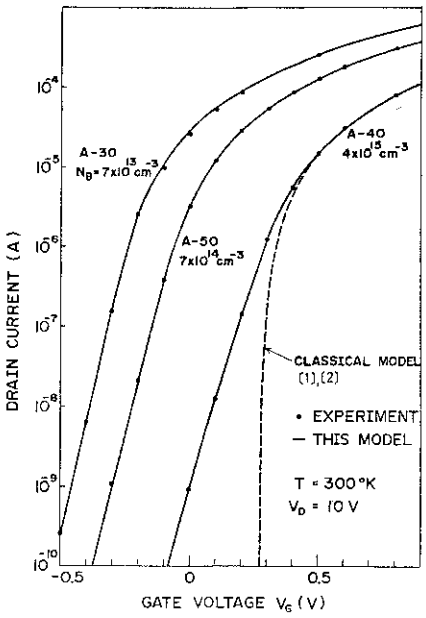


Figure 3.2 Comparison of the model and experiments of the log I_D-V_G characteristics in samples having 675-Å oxide thickness.

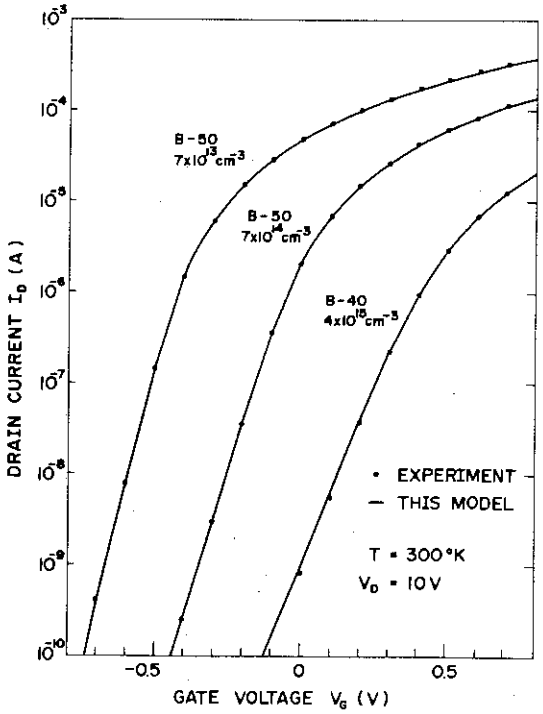


Figure 3.3 Comparison of the model and experiments of the log I_D-V_G characteristics in samples having 1470-Å oxide thickness.

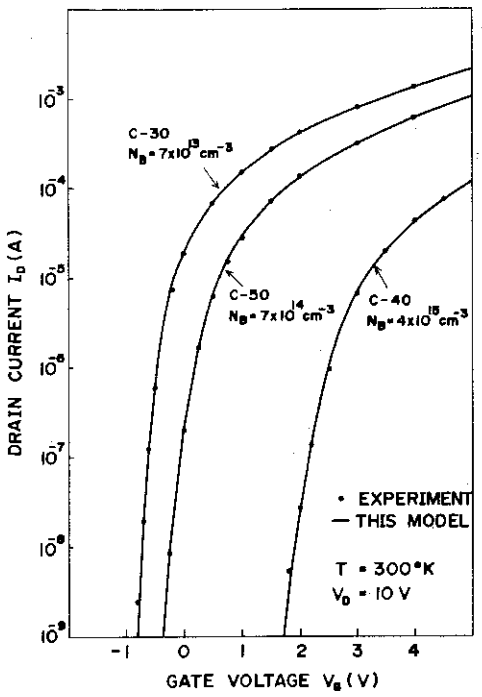


Figure 3.4 Comparison of the model and experiments of the log I_D-V_G characteristics in samples having 5030-Å oxide thickness.

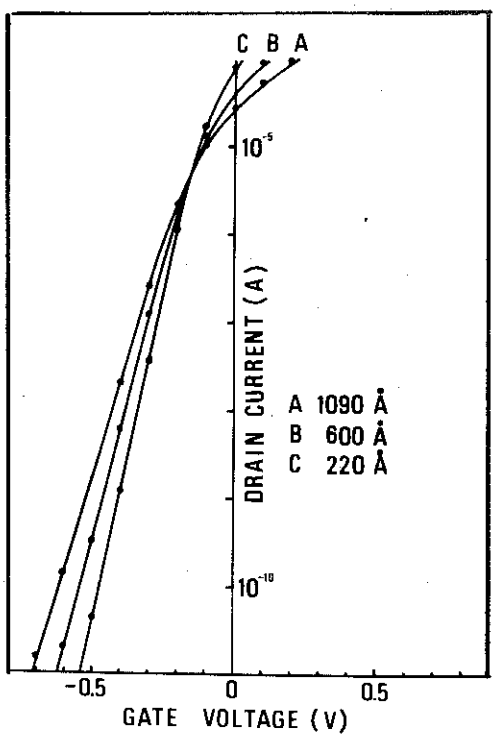


Figure 3.5 Comparison of the model and experiments of the log I_D-V_G characteristics in samples with oxide thicknesses ranging from 220 to 1090 A.

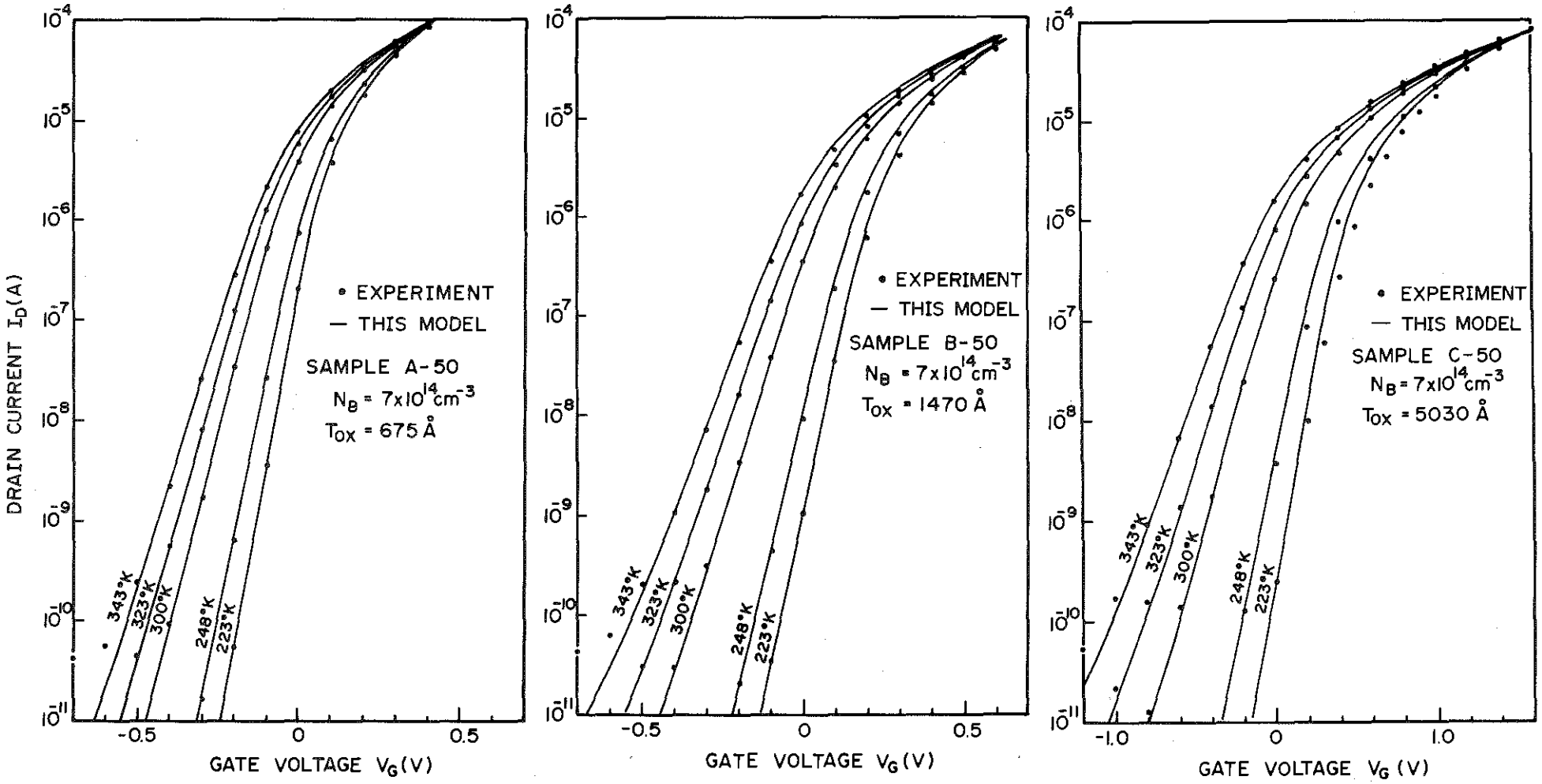


Figure 3.6 Comparison of the model and experiments of the log I_D-V_G characteristics with temperature as a parameter.

Figure 3.7 shows the log I_D - V_D characteristics at room temperature. Disagreement between the theory and the measurement is seen near the pinch-off voltage, that is the boundary between the nonsaturation and the saturation regions; for instance, $V_D = 0.1$ V for $V_G = 0.1$ V, and $V_D = 0.25$ V for $V_G = 0.3$ V. This arises from the approximation of the relationship between the surface potential U_{SF} and quasi-Fermi potential near the pinch-off point. The transition from the nonsaturation region into the saturation region is gradual in actual cases.

Log I_D - V_D curves were measured for all the samples listed in Table 3.2. It was found that the agreement is basically the same as in Fig. 3.7, thus, those figures are not shown here.

The comparison of the model with experiments at higher current levels is shown in Fig. 3.8, where (current in the saturation region or in the tail current region)$^{\frac{1}{2}}$ is plotted as a function of the gate voltage. The agreement is again good. In the figure, some of the marked features of the present model are observed. Taking the sample B-50 as an example, let us explain the features of the curves. When $V_G \geq -0.1$ V, the transistor operates in the saturation region and the (current)$^{\frac{1}{2}}$ is almost in linear relationship with the gate voltage V_G except at high gate voltage region where the mobility decreases. When $V_G < -0.1$ V, the transistor is in the tail current region, and the "tail" is clearly seen in the figure. The arrows in the figure indicate the gate voltage when the surface potential U_{S1} is equal to $2U_F$, that is the threshold voltage above which Eq. (3.32) and (3.35) are valid and below which Eq. (3.29) is valid. Reddi-Sah model is a good approximation when the surface potential is several (kT/q) above $2U_F$, however, it fails below a current level of several microamperes. It should be noted that the threshold voltage defined by Eq.(3.23) does not coincide with the extended threshold voltage from the linear region of (current)$^{\frac{1}{2}}$ - V_G curves, that is the definition of the threshold voltage in the classical models.

It should also be noted that even in the saturation region just above the threshold, the $(\text{current})^{\frac{1}{2}}$ - V_G curves are not straight. This indicates that the variation of the surface potential or the variation of the effective threshold should be taken into account exactly in the strong inversion condition. It was found that significant error is produced in the classical models just above and below the threshold voltage because they exclude the diffusion current and they assume that the surface potential is pinned to $2U_F$.

Figure 3.9 shows electron mobility obtained from the fitting of the calculated curves to the measurements for various samples. These values are taken at the limit of low gate field so that the effect of parameter θ_a is neglected. It has been assumed empirically that mobility is constant at low gate field. This assumption appears to be valid from the various comparisons discussed so far in the preceding paragraphs. The assumption is theoretically supported by Brews [35], in that it has been shown that if the surface state density is low, mobility at weak inversion condition is almost constant with respect to the gate voltage,

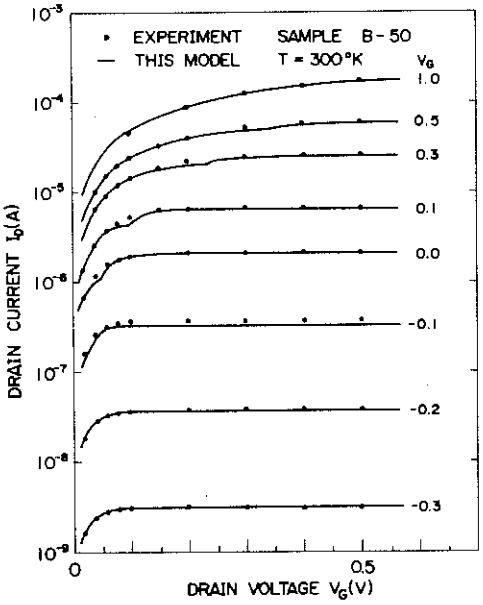


Figure 3.7 Comparison of the model and experiments of the log I_D-V_D characteristics.

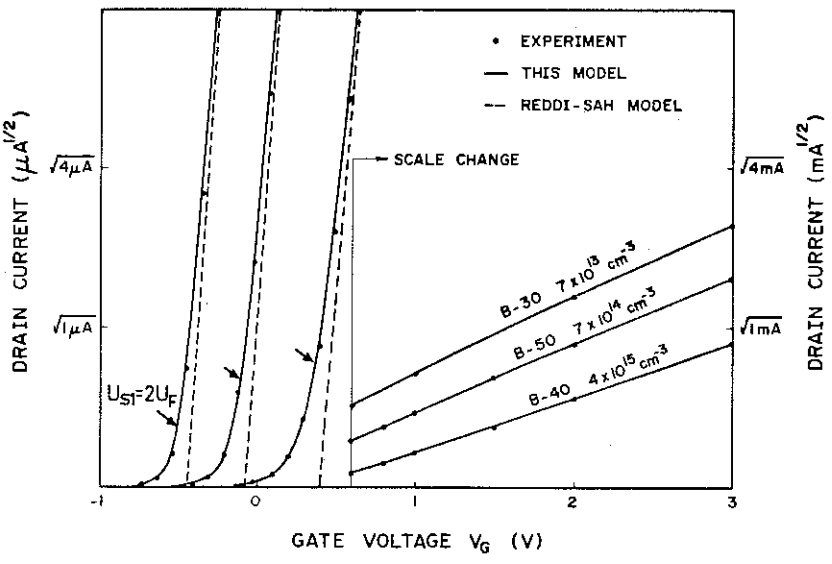


Figure 3.8 Comparison of the model and experiment of the $(I_D)^{\frac{1}{2}}$ - V_G characteristics.

whereas at relatively high surface state density, the localized surface state distribution would produce a decrease of mobility in the weak inversion region. In the figure, the electron mobility obtained from the fitting of this model to the measurements is shown as dots, and the circles and the squares indicate the mobilities obtained from the fitting of Hofstein model and Reddi-Sah model to the measurements of the samples with 1470 Å gate oxide thickness. Other points are left out to avoid confusion. It is seen that a higher value of mobility as compared to that of Hofstein model and Reddi-Sah model is required to fit the present theory to the measurements. This is because U_{Sl} in Eqs. (3.20) and (3.21) is an increasing function of U_G, even if U_{Sl} is larger than $2U_F$, whereas U_{Sl} is assumed to be pinned to $2U_F$ in the other models. In other words, the variation of the "effective threshold voltage" taken in the present theory needs higher mobility. In Fig. 3.9, it should be remarked that the value of mobility in this model coincides with the solid curve that indicates electron mobility in p-type bulk silicon. [36] This in turn indicates that physically accurate value of mobility can be used in the present theory owing to the fact that second order approximations are included in the current expressions.

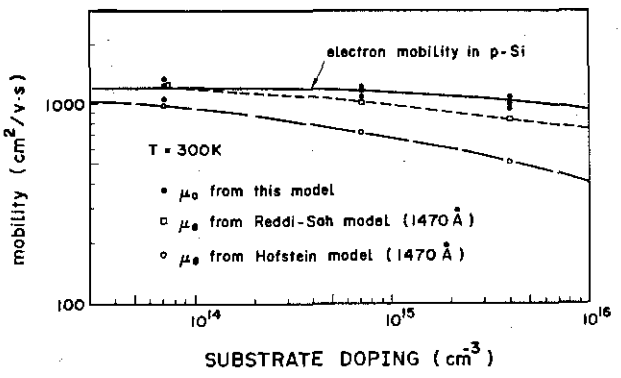


Figure 3.9 Electron mobility versus substrate impurity concentration.

3.3.4 Applications to Circuit Design

In this section, two circuit examples are discussed in which the low-level current has an important influence on the circuit characteristics. First, let us take an enhancement-load static inverter circuit as an example. The circuit schematic and V_{OUT} - V_{IN} dc-transfer curves are shown in Fig. 3.10. In the figure, the experimental results are compared with the calculation using Reddi-Sah model and the model described in this section. The devices have low threshold voltage so that the circuit would operate at 1.5 volts. It is seen that at the shoulders of the transfer curves, "rounding effect" takes place. This is caused by the tail current of the driver(amp) transistor when it is biased below the threshold. Significant decrease of the high level noise margin is observed especially at low supply voltages. It should also be noted that the gain of the circuit, the slope of the transfer curve at the transition region, is somewhat lower in the present model and in the experiments than that expected from Reddi-Sah model. In the limit of very large beta ratio β_R, Reddi-Sah analysis will predict an infinitive gain. However, this is not true because, for very large load resistance, the driver transistor operates in the tail current region where g_m varies in proportion to the current level. Consequently, the limiting value of the gain is observed. This value is determined by the slope of the log $I_D - V_G$ curve and the supply voltage, if the drain conductance in the saturation region is small enough. As seen in the figure, the present analysis is capable of handling these second order effects.

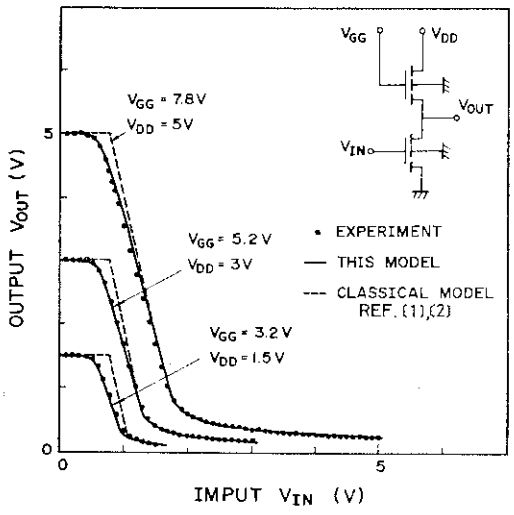


Figure 3.10 E/E inverter dc-transfer characteristics calculated from the present theory and the classical theory.

Figure 3.11 illustrates a typical 3-MOS type memory cell configuration. Storage of the charge in the memory cell is done by first applying a high voltage at the write address and transferring the charge from the data line to the memory capacitor. In the standby mode, the write address should be kept low so that the charge stored across the capacitor C_M does not leak away. The transistors Q_S and Q_R are the sense and the read switch MOSFETs. These transistors are eliminated in a 1-MOS type memory cell. However, the basic mechanism of the memory function is common for both memory cells. In these memory cells, if the transistor Q_W is biased in the tail current region that is below the threshold voltage, stored charge is lost. Thus, the storage time of the cell is strongly influenced by the threshold voltage of the write transistor. The calculated refresh time of the memory at 70 °C is shown in Fig. 3.12 as a function of the threshold voltage at room temperature for various substrate dopings and oxide thicknesses. It is seen that the low limit of the threshold voltage is determined by the tail current. It should be noted that the threshold voltage tolerance is large when a low doped substrate and a thin gate oxide are chosen. The threshold control techniques such as substrate bias or ion-implantation should be applied carefully by taking this into account.

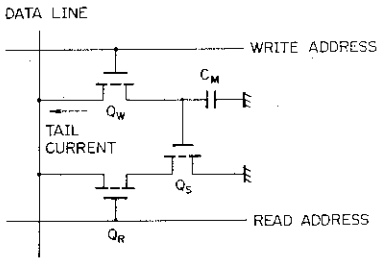


Figure 3.11 Circuit schematic of a typical 3MOS memory cell.

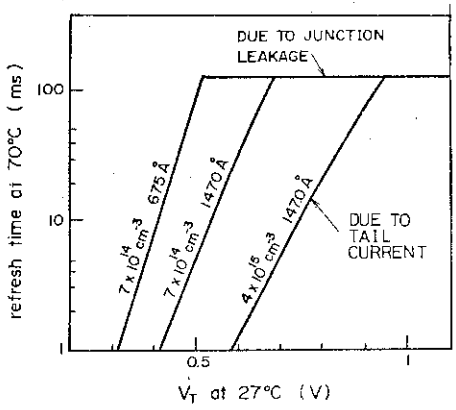


Figure 3.12 Refresh time of the memory cell as a function of the threshold voltage. The limit due to the tail current is calculated from the model and that due to junction leakage is a typical experimental result.

The preceding discussion suggests that it will be convenient to define a voltage ΔV_G as denoting a gate voltage variation that corresponds to one order variation of the drain current. In other words, ΔV_G is the voltage that is inversely proportional to the slope of the log I_D - V_G curve in the tail current region. Although the slope is almost constant, it still has a slight dependence on the current level. In Fig. 3.13, ΔV_G evaluated at 10^{-8} to 10^{-9} A is shown as a function of T_{OX} and with N_B as a parameter. Figure 3.14 shows the temperature dependence of the ΔV_G. Let us evaluate the tail current using these figures. In the first place, we assume that the threshold voltage is defined at a current level of one microampere for the sake of convenience, and that the given threshold is one volt. We also assume that the leakage current should be less than 10^{-10} amperes in a memory cell. If a transistor with a doping of 10^{15} cm^{-3} and a gate oxide thickness of 1200 Å is chosen, and it is operated at 70°C, it follows that the gate voltage at 10^{-10} A becomes, (1V) - (4 × 0.12 V) = 0.52 V. This means that the gate voltage should be kept to less than 0.52 volts at any time to prevent the leakage current to flow.

The value of ΔV_G increases with increasing the gate oxide thickness, substrate doping density and the temperature. Therefore, a special precaution is needed for the tail current in such cases.

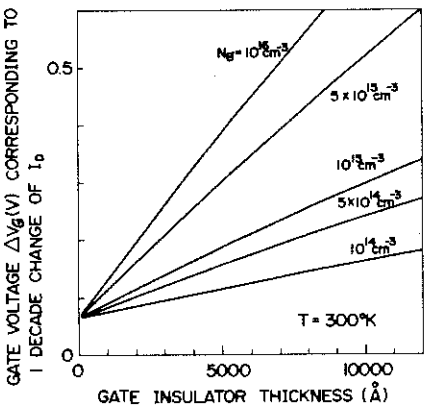


Figure 3.13 ΔV_G versus gete oxide thickness.

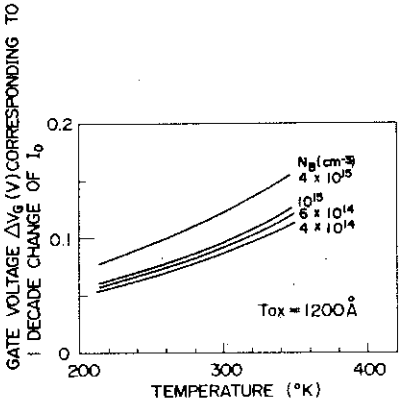


Figure 3.14 ΔV_G versus temperature.

3.3.5 Conclusion

A new model for standard type MOSFET, that handles the drain current above 10^{-10} amperes at 340 K and above 10^{-11} amperes below 320 K, was proposed. Surface potentials at the source end and at the pinch-off point were used as explicit parameters in the current expressions for the purpose of obtaining a natural connection in the tail current and the saturation regions. The current expressions are analytical and is suitable for computer analysis of the circuits, especially it is a convenient tool to analyze various second order effects caused by the low-level currents in MOSFET.

Comparison of the model with the measurements was performed using n-channel Al gate and Si gate transistors with substrate doping densities ranging from 7×10^{13} cm^{-3} to 4×10^{15} cm^{-3}, and oxide thicknesses ranging from 220 Å to 5030 Å. Although a slight deviation was observed near the pinch-off voltage that arises from the approximation of the model, the calculated points were in good agreement with the measurements. Thus, the proposed model was proved to be applicable to actual circuit design throughout the entire region of operation of MOSFET.

To demonstrate several examples to apply the model, the influence of the low-level tail current on static E/E (enhancement/enhancement) type inverter circuit and the dynamic memory cell was studied. Generally, the tail current should always be considered in the circuits that operate at low voltages, in a dynamic mode and at a high temperature.

Some problems left for further study are; a smooth connection of the current equations between the nonsaturation and the saturation regions, and to include the channel length modulation effect and the threshold variation due to the drain voltage and the channel length in a short channel device.

3.4 SUBTHRESHOLD CURRENTS IN ION-IMPLANTED MOSFET [45], [46], [47]

3.4.1 Introduction

Ion-implantation for threshold voltage control has become widely accepted in MOSIC fabrication. Its advantage is that it permits a threshold shift over a wide range both positively and negatively. This allows the fabrication of a p-channel depletion type MOSFET, an n-channel enhancement type MOSFET and a channel stopper for field region which can not be made without the use of ion-implantation.

Many reports have been published on the threshold shift by ion-implantation. Aubuchon [37], Coppen [38], Swanson and Meindl [29], and Sigmon and Swanson [39], have given analytical expressions for the threshold shift. Brotherton and Burton [40], Tanaka [41], MacPherson [42], and Warabisako, Yoshida and Tokuyama [43] have explained the threshold shift by numerical calculations of the potential profile in ion-implanted silicon substrates. At the same time, Moline and Reutlinger [44] have given some experimental data for the threshold shift of MOSFET having double-implanted layers.

As has been discussed in Section 3.3, due to the recent advances of MOS circuit techniques, a leakage current of an order of a nanoampere has become important. Thus, special precautions should be taken associated with the low-current level characteristics of MOSFET. It has been pointed out in the preceding section that in the case of a uniformly-doped MOSFET, a design including the "tail current" is required. In ion-implanted MOSFET, the tail in $(I_D)^{\frac{1}{2}} - V_G$ curve is significantly affected by the implantation conditions. Furthermore, in deep depletion type MOSFET, a "residual current" is observed even when the gate bias is well below the threshold voltage. Therefore, the low-current-level characteristics are quite different from those in standard type MOSFET.

In this section, these low-level currents in ion-implanted MOSFETs are studied. The discussion is based on the numerical calculation of the potential profile and electron and hole densities in one dimension. Some experimental results will also be shown. Sections 3.4.2 and 3.4.3 discusses the numerical calculation method and its accuracy. Section 3.4.4 gives a discussion on low-level currents in a MOSFET having a single implanted layer. Section 3.4.5 deals with double layer implantation conditions for the purpose of controlling both the threshold voltage and the low-level currents independently.

3.4.2 Numerical Analysis Method

Poisson's equation for a semiconductor substrate with an implanted impurity distribution $N_{IMPL}(x)$ is given by

$$\frac{d^2U}{d\chi^2} = -\frac{q}{\epsilon_S}\frac{q}{kT}[P - N + N_D - N_A \pm N_{IMPL}(\chi)] \quad , \tag{3.38}$$

where U is the potential in the unit of (kT/q). Electron concentration N, hole concentration P, acceptor and donor concentrations N_A and N_D are expressed by

$$P = N_I \exp(U_F - U) \tag{3.39}$$

$$N = N_I \exp(U - \xi - U_F) \tag{3.40}$$

$$N_A = N_I \exp(U_F) \tag{3.41}$$

$$N_D = N_I \exp(-U_F) \quad . \tag{3.42}$$

According to LSS theory [48], the implanted impurity profile can be approximated by a Gaussian distribution. However, Gibbons et al. [49] have pointed out that the real distribution exhibits a profile including the third central moment and can be approximated by so called "joined half Gaussian". This is given by two joined Gaussians having different standard devia-

tions as seen by the equations,

$$-\infty < \chi \leq R_M : N_{IMPL}(\chi) = \frac{2N_{DT}}{(2\pi)^{1/2}(\sigma_1 + \sigma_2)} \exp\left[-\frac{(\chi - R_M)^2}{2\sigma_1^2}\right] \qquad (3.43)$$

$$R_M < \chi < \infty : N_{IMPL}(\chi) = \frac{2N_{DT}}{(2\pi)^{1/2}(\sigma_1 + \sigma_2)} \exp\left[-\frac{(\chi - R_M)^2}{2\sigma_2^2}\right] , \qquad (3.44)$$

where N_{DT} is the total ion-dose, R_M is the position at the peak of the distribution, and σ_1 and σ_2 are the standard deviations in the left half and the right half of the distribution.

Equation (3.38) can be numerically solved if the value of quasi-Fermi potential ξ is given. The boundary conditions are

$$\chi = -T_{OX}: \quad U = U_G \qquad (3.45)$$

$$\chi = 0: \quad \epsilon_S(dU/d\chi)_{+0} = \epsilon_{OX}(dU/d\chi)_{-0} \qquad (3.46)$$

$$\chi = \infty: \quad U = 0. \qquad (3.47)$$

The numerical calculation of Eq. (3.38) is carried out by the over-relaxation method in one dimension as seen in Fig. 3.15. The over-relaxation constant ω is selected to be 1.6 to 1.8, and the mesh size h_i is 2 Å at the surface of silicon and is gradually increased according to the equation $h_i = \alpha h_{i-1}$ where α = 1.1 to 1.2. These values are carefully chosen so that the convergence is obtained for any cases. The calculation is done up to a depth of 5 μm that corresponds to the maximum mesh number n_{max}. The potential profile calculation is performed until the condition $|U_{i,k} - U_{i,k-1}| < \epsilon$ is satisfied, in which $\epsilon = 10^{-3}$ for the calculation of induced mobile charge n_{SF} and $\epsilon = 2 \times 10^{-5}$ for the calculation of the capacitance vs. voltage curves.

Once the potential profile is calculated, the corresponsing surface electron density $n_{SF}(\xi)$ is calculated by performing the integration,

$$n_{SF}(\xi) = \int_0^{x_D} N_I \exp(U - \xi - U_F)\, d\chi \qquad (3.48)$$

where x_D is the depth at which the electron density is equal to the hole density.

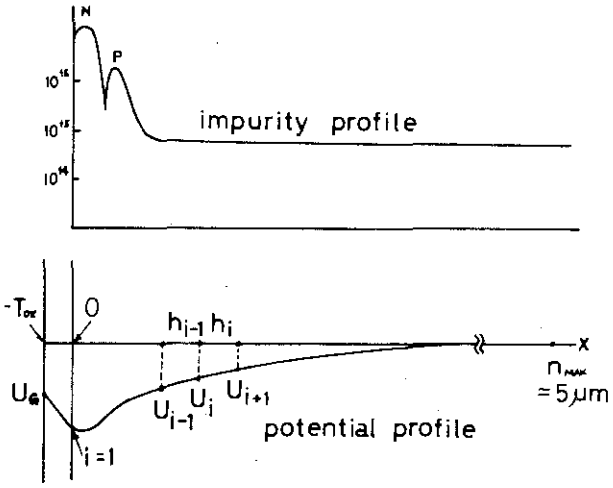


Figure 3.15 Mesh points and boundary conditions for the numerical calculation of potential and charge.

The drain current can be obtained by performing the integral (3.17). However, this needs a calculation of double integral and thus requires a long computer time. In this section, the surface electron density at the source $n_{SF}(U_S)$ is chosen to discuss the low-level currents. The reason for this is as follows. In the preceding section it was shown that $n_{SF}(U_S)$ is in proportion to the drain current both in the tail current region and in the nonsaturation region for unimplanted cases. First, in the tail current region, and when $U_D \gg 1$, Eq. (3.30) can be rewritten as

$$I_D = W\mu \left(\frac{kT/q}{L}\right) q n_{SF}(U_S). \qquad (3.49)$$

For the nonsaturation region, and when U_D is small

$$I_D = W\mu \left(\frac{V_D}{L}\right) q n_{SF}(U_S). \qquad (3.50)$$

This means that $n_{SF}(U_S)$ is proportional to the drain current in both regions, and the multiplication factors are equal provided $U_D \gg 1$ in the tail current region and $U_D = 1$ in the nonsaturation region are assumed.

3.4.3 Numerical Calculation Accuracy

Numerical calculation accuracy was checked as follows. First, a comparison of the potential profile, log $n_{SF} - V_G$ curve and the low frequency capacitance vs. voltage curve between the numerical calculation and the theoretical analysis using F-function [50] was made for unimplanted cases. Second, the numerical calculation of log $n_{SF} - V_G$ curve was compared to the measurements for implanted cases.

Figure 3.16 shows the comparison of the low frequency C-V curve for an unimplanted case. The calculated points from this analysis are obtained by using the equation,

$$C = C_{ox}\left(1 - \frac{\Delta U_{SF}}{\Delta U_G}\right) , \qquad (3.51)$$

where ΔU_{SF} is the difference of the two surface potentials that correspond to the gate voltages $U_G + \Delta U_G/2$ and $U_G - \Delta U_G/2$. In

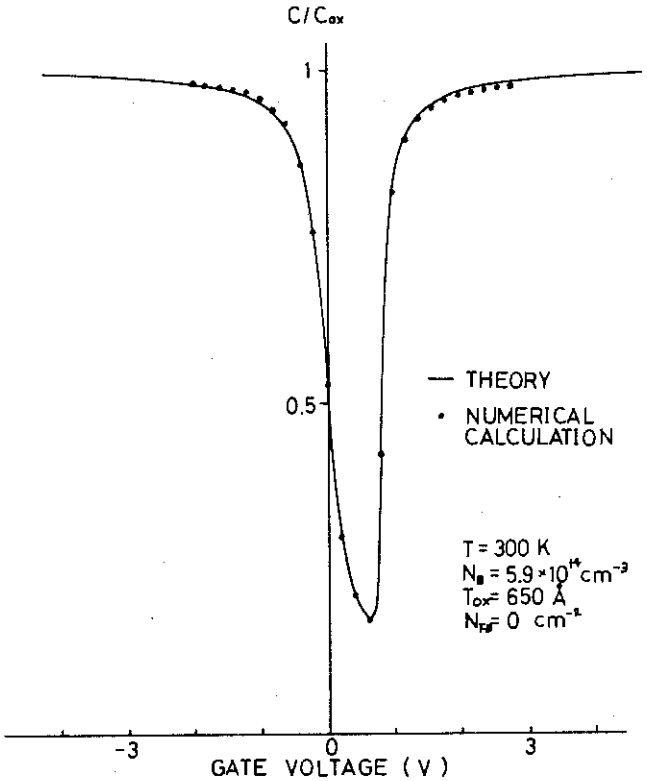


Figure 3.16 Comparison of the low-frequency capacitance-voltage curve between the numerical calculation and theoretical analysis using F-function for an unimplanted case.

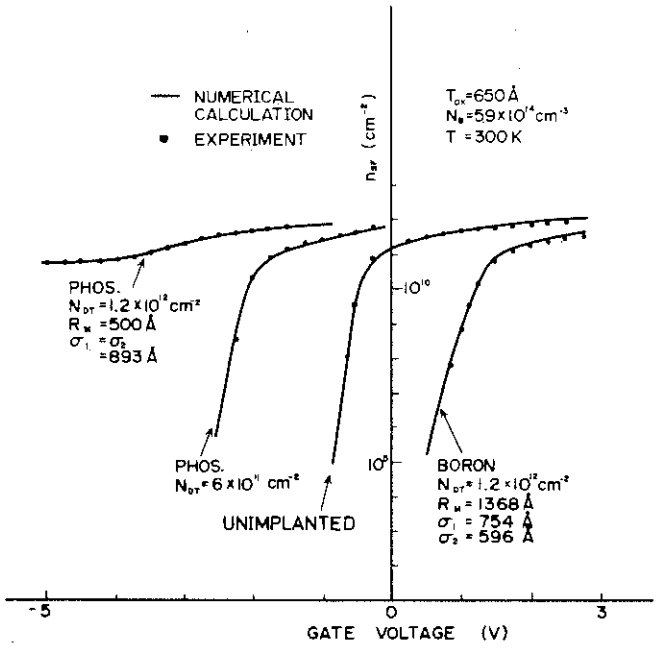


Figure 3.17 Comparison between numerical calculation and experiments of log n_{SF}-V_G curves.

Fig. 3.16, slight disagreement is seen when $C/C_{OX} > 0.9$. Otherwise, the numerical calculations are in excellent agreement with the theoretical points.

Figure 3.17 shows the comparison of the log n_{SF} - V_G curves between the numerical calculation and the experimental measurements for both unimplanted and implanted MOSFETs. The implanted MOSFETs have either single boron or phosphorus layer. The experimental results were obtained by measuring the drain current at a drain voltage of 30 mV and by substituting the values into Eq. (3.50). This might cause some error in the tail current region because the current obeys Eq. (3.49). Actually this does not produce a significant error as far as we discuss the current behavior in a logarithmic scale. Therefore, it is used for convenience. From Fig. 3.17, we can conclude that the present calculation gives a good approximation for the number of the induced electrons, that means that the low-level currents in MOSFETs are accurately predicted by this analysis program.

3.4.4 Low-Level Currents in MOSFET with a Single-Layer Implantation

Figure 3.18 shows log n_{SF} - V_G curves in boron implanted n-channel MOSFETs. The parameters are ion-dose and the depth. When the depth is shallow, as shown in Fig. 3.18 (A), only the distribution tail within the silicon substrate contributes to the shift of the curves. Therefore, the amount of the threshold shift is relatively small and almost a parallel shift of the curves is obtained. However, when the dose is high and when the peak of the impurity is well into the substrate, the threshold shift is not proportional to the amount of the impurity within the substrate and a saturation of the shift is seen. It is also noted that the slope of the log n_{SF} - V_G curves tends to become less steep in the case of a high dose.

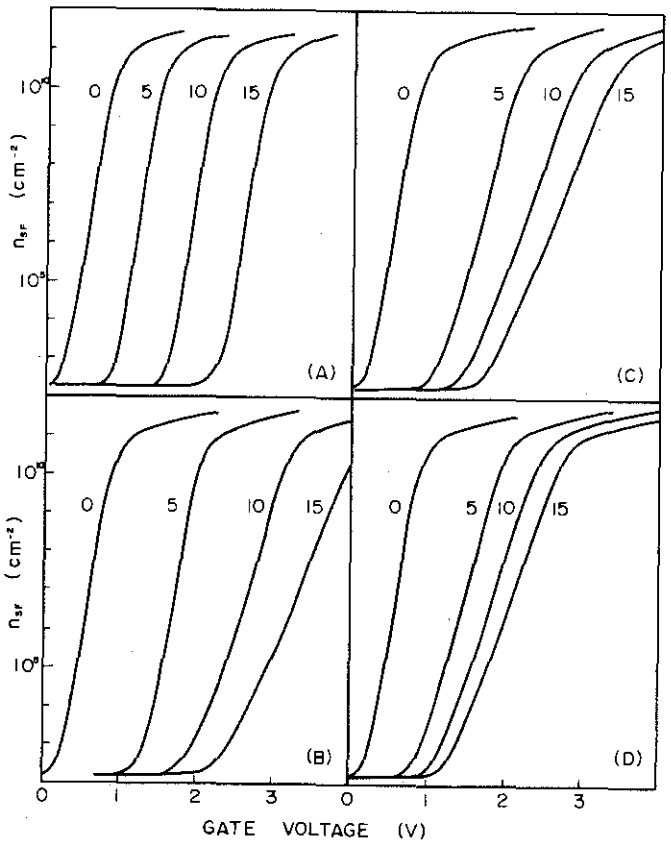


Figure 3.18 Calculated shift of log n_{SF}-V_G curve due to single-layer boron implantation. (A) R_M=−24 Å, $\sigma_1=\sigma_2$=321Å, (B) R_M=390Å, $\sigma_1=\sigma_2$=439Å; (C) R_M=800Å, $\sigma_1=\sigma_2$=538Å; (D) R_M=1220Å, $\sigma_1=\sigma_2$=627Å; N_{DT}($\times 10^{11}$cm^{-2}), $N_B=5.9\times10^{14}$cm^{-3}, T_{ox}=650Å, T=300K.

Figure 3.19 illustrates the variation of the potential profiles for various implantation depths. In the case of a shallow implantation, the implanted impurity exists in the surface depletion region and inversion region. This means that the slope of the log n_{SF} - V_G curve in the tail current region is determined by the impurity concentration of the substrate. On the other hand, in the case of deep implantation, the surface depletion layer is shielded by the implanted layer. This in turn means that the impurity concentration at the edge of the surface depletion layer is high. This situation is similar to the case where a substrate having a high boron concentration is used. For this reason, less steep log n_{SF} - V_G curves are observed in such cases.

Figure 3.20 illustrates log n_{SF} - V_G curves for phosphorus or arsenic implanted n-channel MOSFET. Figure 3.21 shows some of the corresponding potential profiles. These species yield a negative threshold shift. When the depth of the implantation is shallow, as shown in Fig. 3.20 (A), the behavior is similar to the case shown in Fig. 3.18 (A), that is, the amount of the threshold shift is small and the shift is almost in a parallel man-

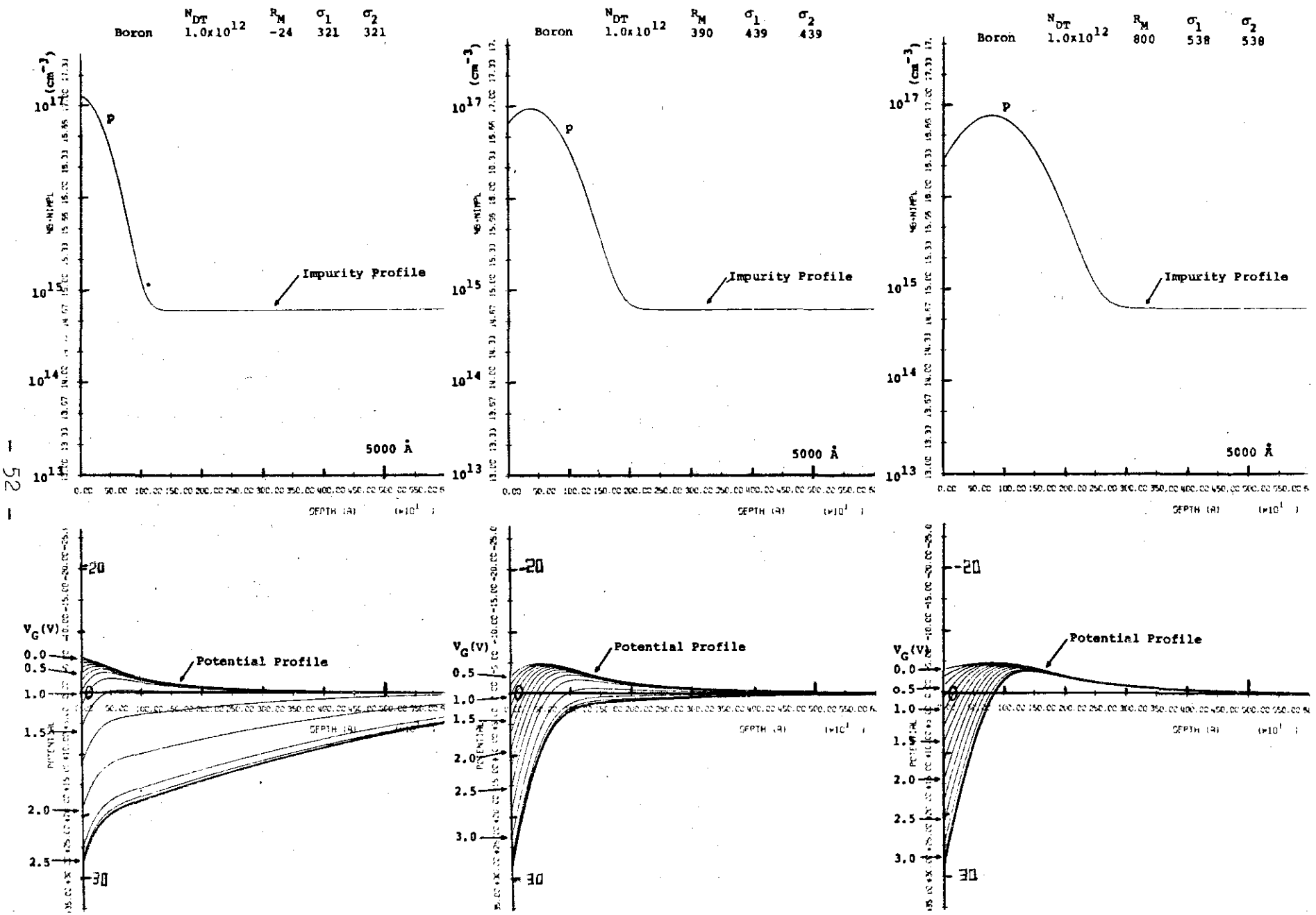


Figure 3.19 Potential profiles for single-layer implantation.

ner. In the case of deep implantation and high dose, the threshold shift does not saturate, that is a quite different behavior as compared to the case of boron implantation. The unique feature seen in the figure is the occurence of the residual current. The residual current is caused by the implanted channel region that is not pinched-off even when a large negative gate voltage is applied. The amount of the residual current is large when the total dose and the depth of the implanted n-layer is large. There have been several reports published on the analysis [29], [53], and experiments [51], [52] of a single layer n-type implantation, and the detailed discussion is not repeated here. It is noted that the residual current in a depletion type load device does not cause a deterioration of the circuit performance in a static mode of operation. There are some applications in which the residual current is advantageous. This will be discussed later.

From the preceding discussions, it was revealed that a delta-function-like implantation yields a parallel shift of the log n_{SF} - V_G curve. This is a desirable situation in n-channel enhancement MOSFET for use in dynamic memory circuit. One possible approach is, as has been shown in Fig. 3.18, a very shallow implantation in that the peak of the ion-distribution is within SiO_2. However this te-

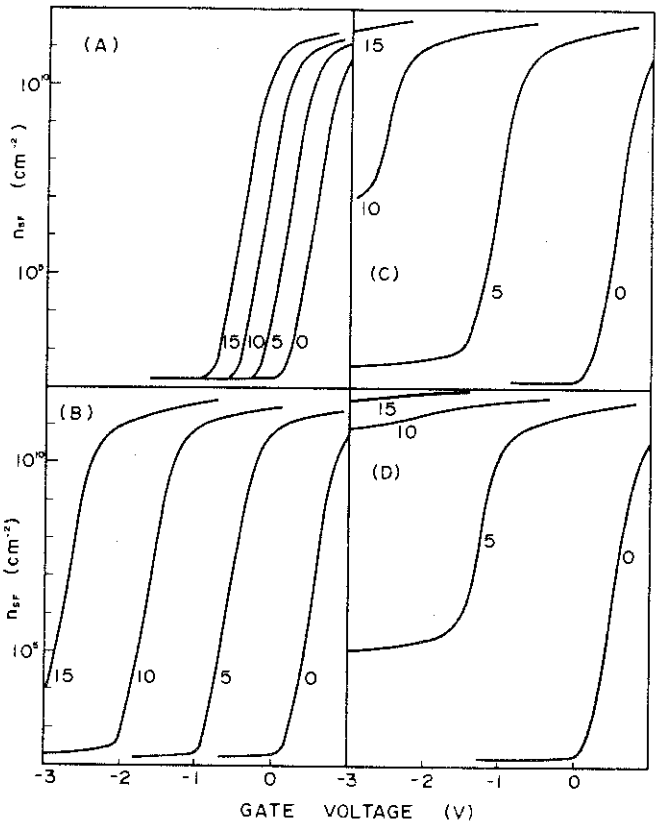


Figure 3.20 Calculated shift of log n_{SF}-V_G curve due to single-layer phosphorus implantation. (A) R_M=−166Å, $\sigma_1=\sigma_2$=198Å; (B) R_M=100Å, $\sigma_1=\sigma_2$=280Å; (C) R_M=410Å, $\sigma_1=\sigma_2$=354Å; (D) R_M=730Å, $\sigma_1=\sigma_2$=426Å; N_{DT}($\times 10^{11}$cm^{-2}), N_B=5.9×$\times 10^{14}$cm^{-3}, T_{ox}=650Å, T=300K.

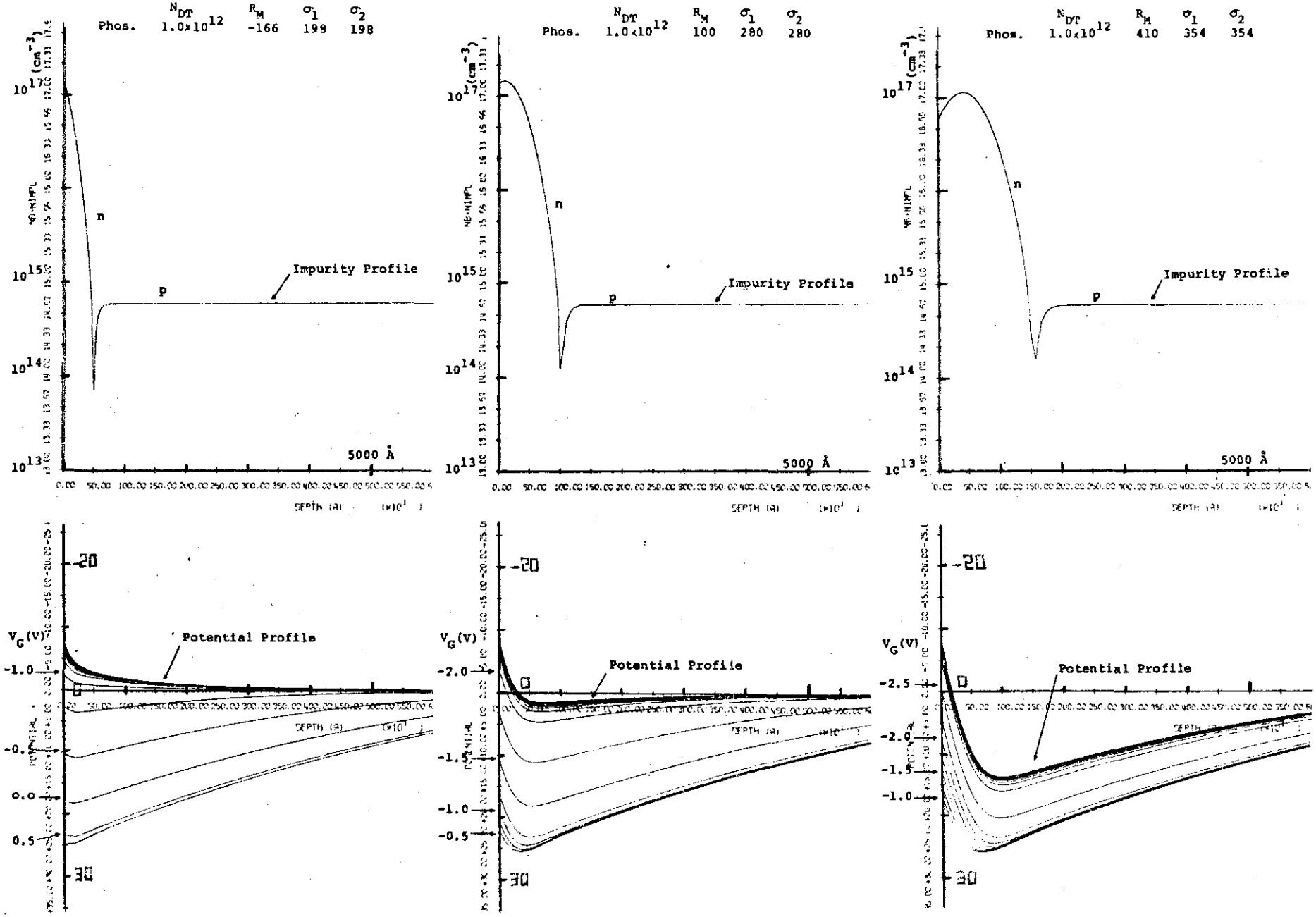


Figure 3.21 Potential profiles for single-layer phosphorus implantation.

chnique is quite sensitive to the variation of the ion energy and oxide thickness and might cause a large variation of the threshold shift. Another possibility is to use arsenic or antimony and to perform ion-implantation prior to the gate oxidation. These impurities have relatively small diffusion constant and thus the shallow distribution made by the implantation without gate oxide does not diffuse too much during the succeeding steps. However, for the typical p-type impurity boron this is not applicable. In view of this, a practical method that makes possible a parallel shift of the log n_{SF} - V_G will be proposed in the next section.

3.4.5 Low-Level Currents in MOSFETs with a Double-Layer Implantation

This section describes the effect of double-layer implantation upon low-current level characteristics of MOSFET. Especially, the emphasis is on the control and the design of the tail current and the residual current. The double-implantation that is discussed in this section is illustrated in Fig. 3.22. Figure 3.23 shows various double implantation conditions that are discussed in this section. The doping profiles and the corresponding potential curves for large positive and negative bias are schematically indicated.

(1) Cases (2) and (5) --- Parallel shift of log n_{SF} - V_G curve

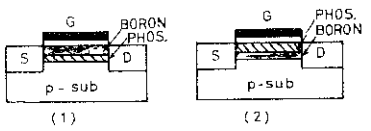


Figure 3.22 Double-layer implanted MOSFET.

Let us first discuss the cases where almost parallel

shift of the log $n_{SF} - V_G$ curves are obtained. As described in the previous section, the potential curves are significantly modified by the implanted impurities, especially when they exist deeply in the substrate because the potential curves can not be controlled by the gate voltage. Thus, it is desirable to have a shallow and delta-function like impurity distribution in order to have a parallel shift of the log $n_{SF} - V_G$ curve. By compensating for the distribution tail of the impurity profile, an equivalent delta-function-like distribution can be realized. In Fig. 3.24, the calculated log $n_{SF} - V_G$ curves for such implantation conditions are shown. These curves correspond to:

(1) single layer implantation,

(2) double layer implantation with $N_{DT1} / N_{DT2} = 10/5$, and

(3) double layer implantation with $N_{DT1} / N_{DT2} = 10/7$.

Total doses are selected so that the shift of the threshold is equal for each case. It is seen that the condition (3) gives the steepest log $n_{SF} - V_G$ curve for the positive threshold shift and the minimum residual current for the negative threshold shift. Figure 3.25 shows the impurity and the potential profiles for these conditions. The figure clearly illustrates the fact that a delta-function-like impurity distribution is realized for the main impurity especially when the ratio N_{DT1}/N_{DT2} is small. The shape of the potential profile is drastically different between the single and the double layer implantations. For example, the depletion layer is shielded by the boron layer in the single layer implantation case shown in Fig. 3.25 (a), whereas the depletion

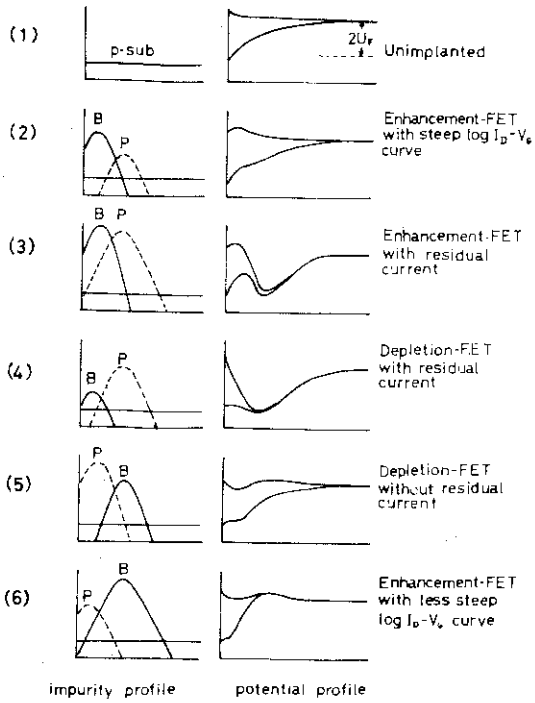


Figure 3.23 Implantation conditions for controlling the tail and the residual currents. Two potential curves in each figure exhibit accumulation and inversion cases.

layer extends to a deeper position in the substrate in the double implantation case shown in (c). For the negative threshold shift, single layer implantation, as shown in Fig. 3.25 (d), yields a deep minimum in the potential profile curve. However, the depth of the minimum is reduced in the double implantation case, and at the same time, the minimum is shifted toward the surface. These features in the potential curve cause the parallel shift of the log $n_{SF} - V_G$ curves.

In order to realize these double implantation conditions, care should be taken first to get a desirable threshold shift. The simple estimation of the shift is given by $\Delta V_T \simeq (q/C_{OX}) \times (N_{DS1} - N_{DS2})$, where N_{DS} is the amount of the implanted impurities into silicon substrate. Second, the amount of the second impurity should not be too much because excess compensation would cause a residual current in an enhancement mode MOSFET, and a less steep log $n_{SF} - V_G$ curve in a depletion mode MOSFET. There are some other possible applications for such conditions, and these will be discussed in the next paragraphs.

	R_M (Å)	$\sigma_1=\sigma_2$ (Å)
P	410	354
B	600	490

	R_M (Å)	$\sigma_1=\sigma_2$ (Å)
B	390	439
P	537	383

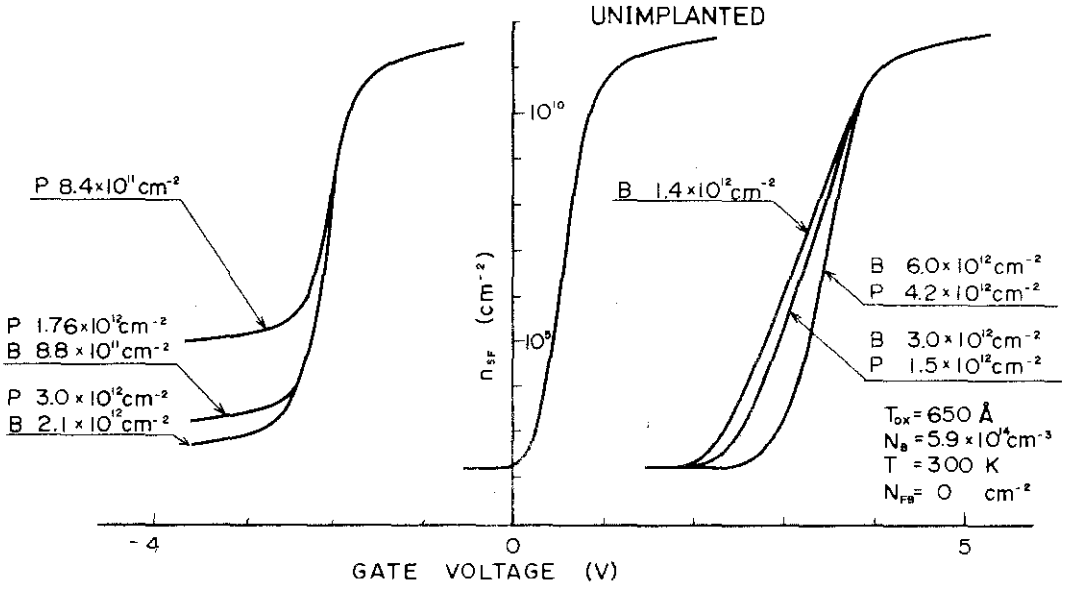


Figure 3.24 Comparison of the shift of log n_{SF}-V_G curve due to single and double-layer impurities. The main impurity is implanted in the surface side.

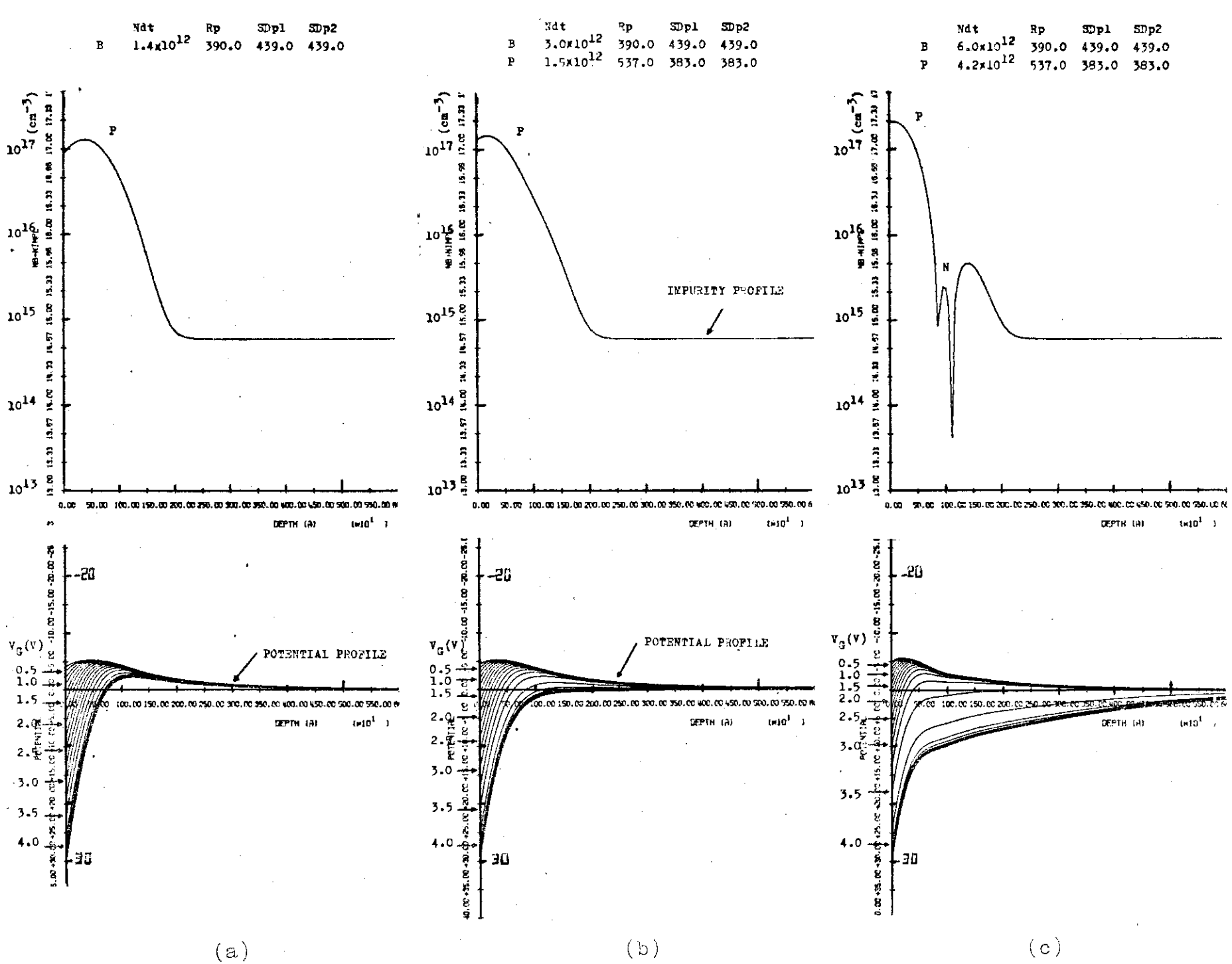


Figure 3.25 Potential profiles for double-layer implanted substrates corresponding to the cases shown in Fig. 3.24.

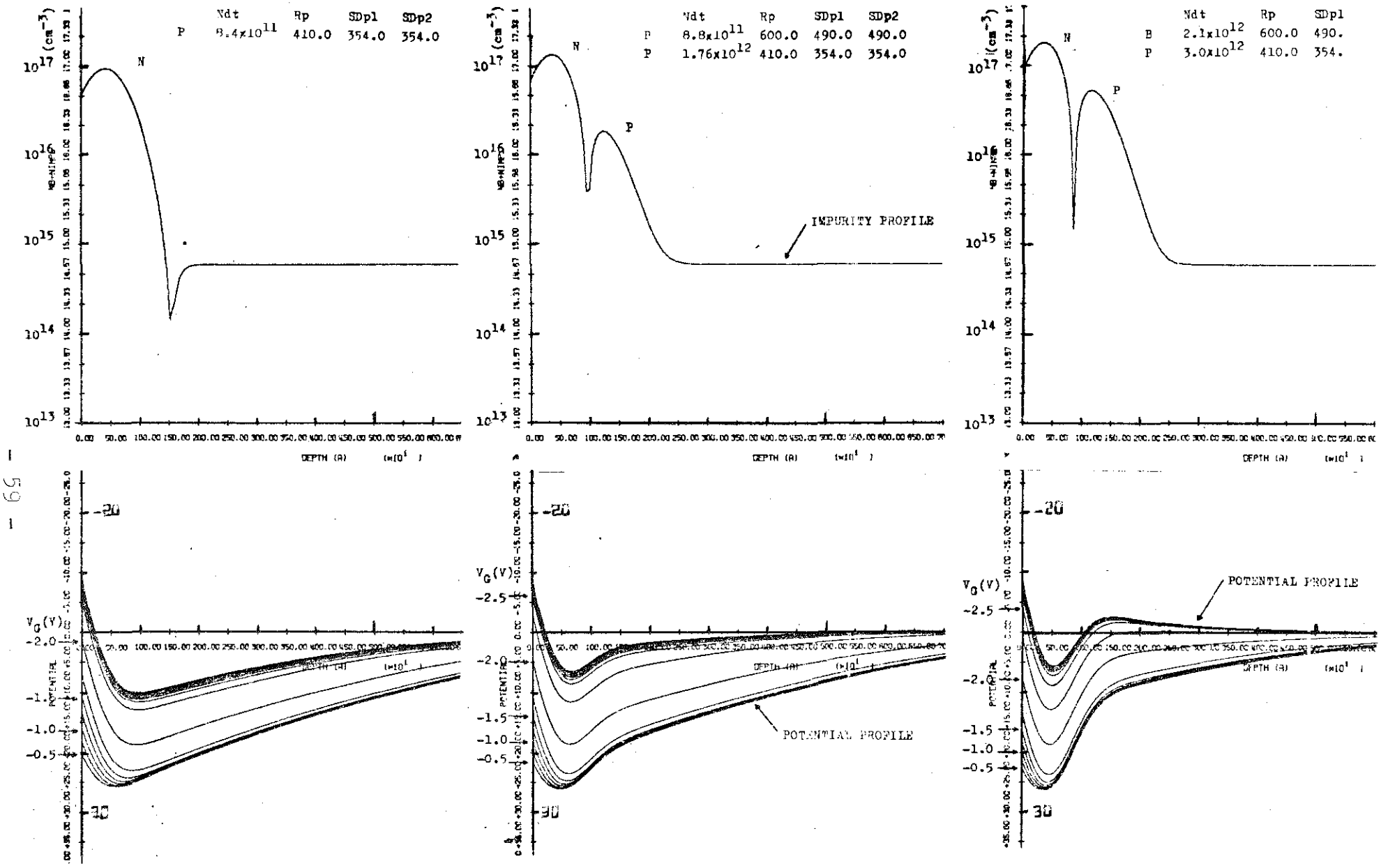


Figure 3.25 Potential profiles for double-layer implanted substrates corresponding to the cases shown in Fig. 3.24.

(2) Cases (3) and (4) ----- MOS transistor with residual current

If the amount of the n-type ions for the second layer is large enough, the n-type ions form a buried channel that can never be pinched-off by the gate voltage. Consequently, MOS transistors with residual current are realized. Two examples of the impurity profiles and the potential profiles for such conditions are shown in Fig. 3.26 and Fig. 3.27. These correspond to enhancement and depletion mode transistors. The shift of the threshold

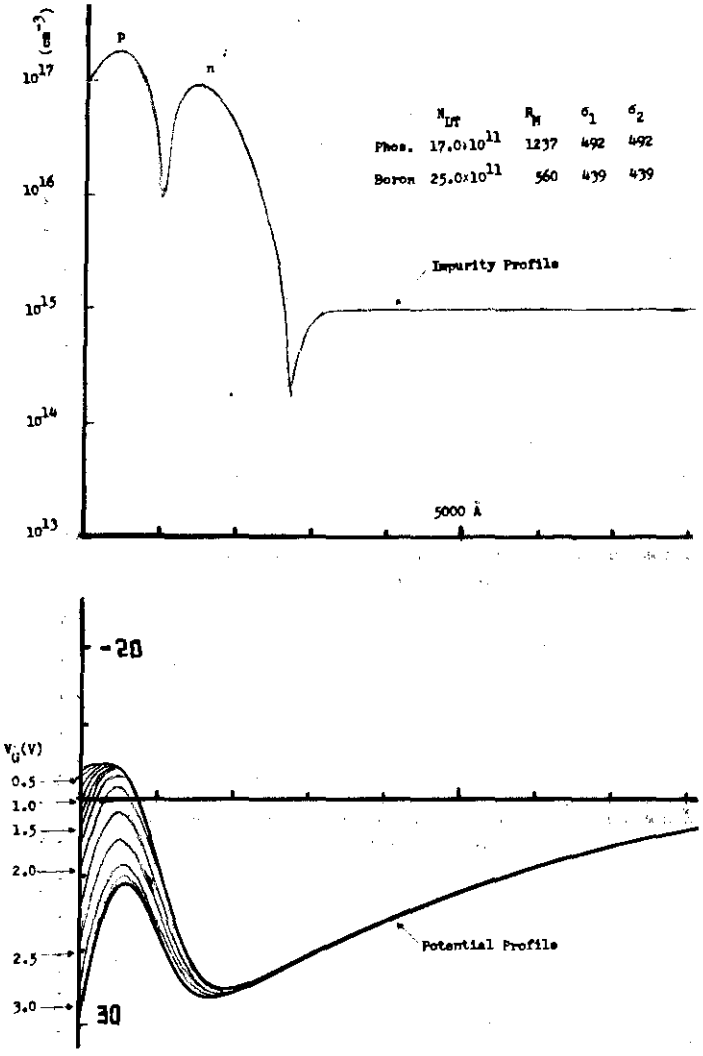


Figure 3.26 Double-layer implantation for the purpose of fabricating an enhancement mode transistor with residual current.

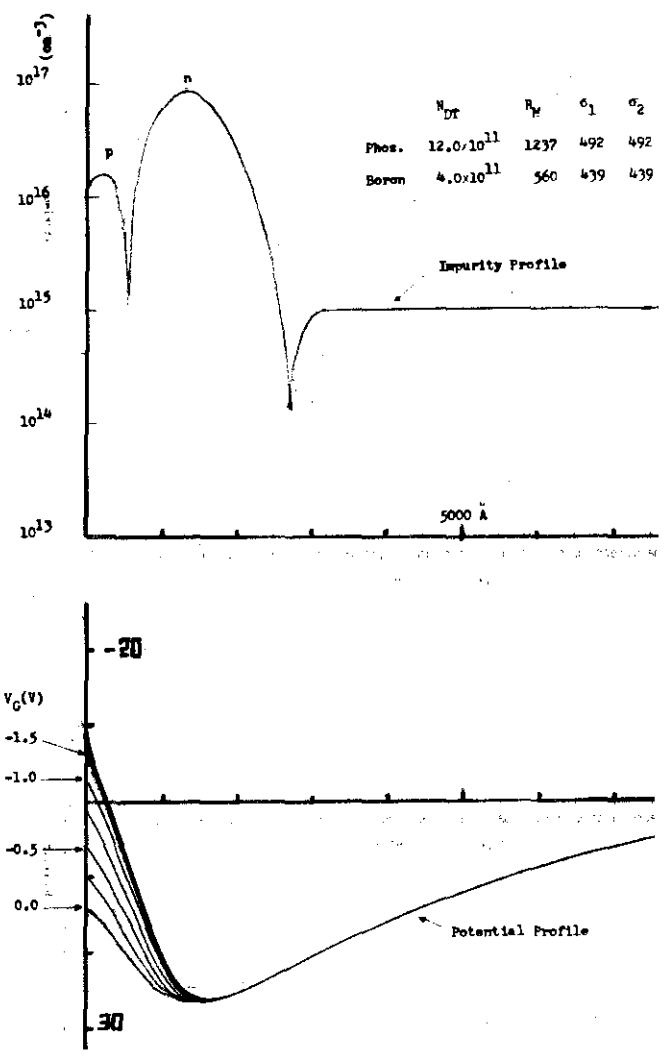


Figure 3.27 Double-layer implantation for the purpose of fabricating a depletion mode transistor with residual current.

is determined by the difference of the doses of two impurities within silicon, as has been stated previously, and the amount of the residual current is determined mainly by the dose of the second n-type layer and the depth. This indicates that it is possible to determine the threshold voltage shift and the residual current independently.

The log $n_{SF} - V_G$ curves for various implantation conditions to design the residual current are shown in Figs. 3.28 and 3.29. It should be noted that the case shown in Fig. 3.28 is obtained when one over-compensates the tail of the first boron layer in order to get an enhancement mode MOS transistor with less steep log $n_{SF} - V_G$ curves.

The MOS transistor having residual current can be used as load devices with a pulse signal at the gate electrode. A typical circuit example is shown in Fig. 3.30. The load transistors used in the flip-flop are designed so that very small residual currents flow when the gate voltages are low. The load pulse goes high only when it is necessary to change the state of the flip-flop. This operation makes possible a very low standby po-

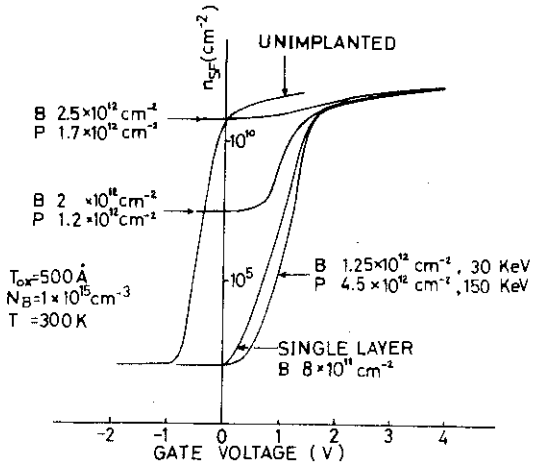


Figure 3.28 Log n_{SF}-V_G curves corresponding to CASE (3) in Fig. 3.23.

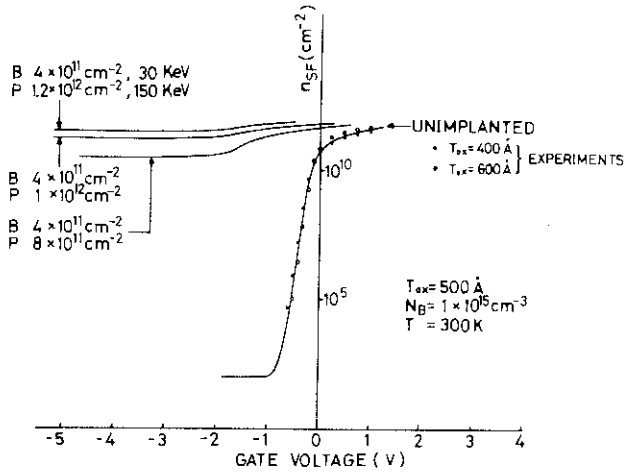


Figure 3.29 Log n_{SF}-V_G curves corresponding to CASE (4) in Fig. 3.23.

wer because it is determined by the residual current of the load transistor and this can be reduced to an order of a nano-ampere. An advantage of this circuit is that it operates in a static mode. The high level voltage of the memory nodes is kept high and the residual current of the load device prevents the high node to be discharged. In other words, the equivalent circuit when the load pulse is low has residual current sources between the supply line and the memory nodes. This is a quite effective way to reduce the power dissipation of the memories and microprocessors while keeping its static operation.

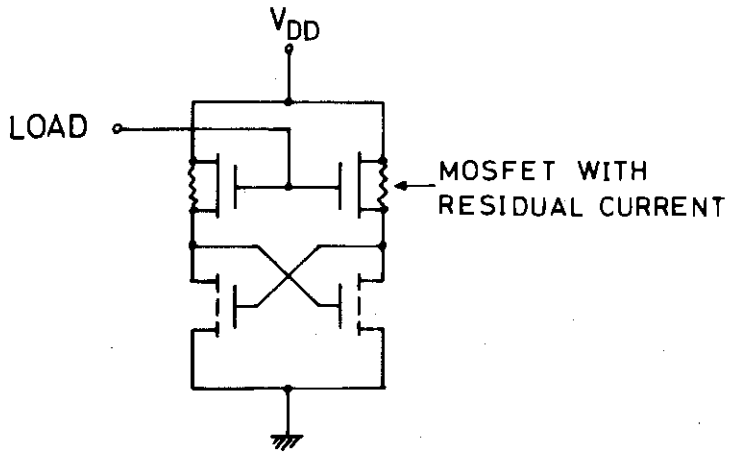


Figure 3.30 A quasi-static latch utilizing MOSFETs with residual current.

(3) Case (6) ---- remote cut-off log $I_D - V_G$ curve

Let us discuss the condition in which boron is implanted deeply into the substrate and the distribution tail near the surface is compensated for by phosphorus or arsenic. The calculated log $n_{SF} - V_G$ curves and the potential curves for these conditions are shown in Figs. 3.31 and 3.32.

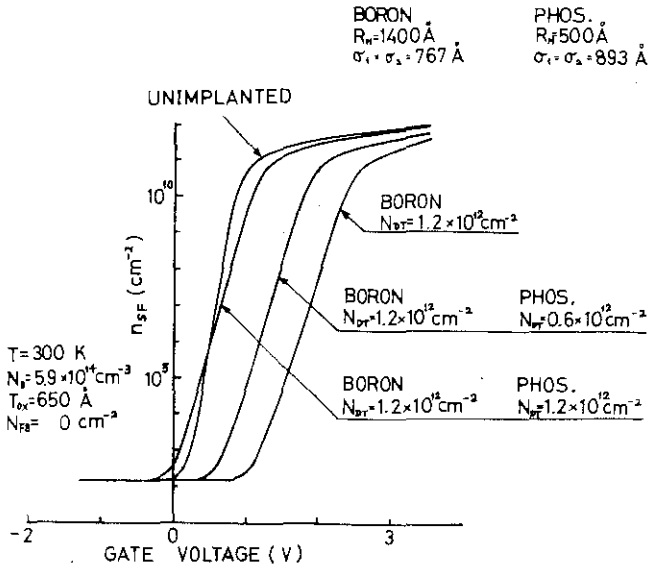


Figure 3.31 Calculated shift of log n_{SF}-V_G curve due to double-layer implantation CASE (6) in Fig. 3.23, where boron is implanted deeply in the substrate.

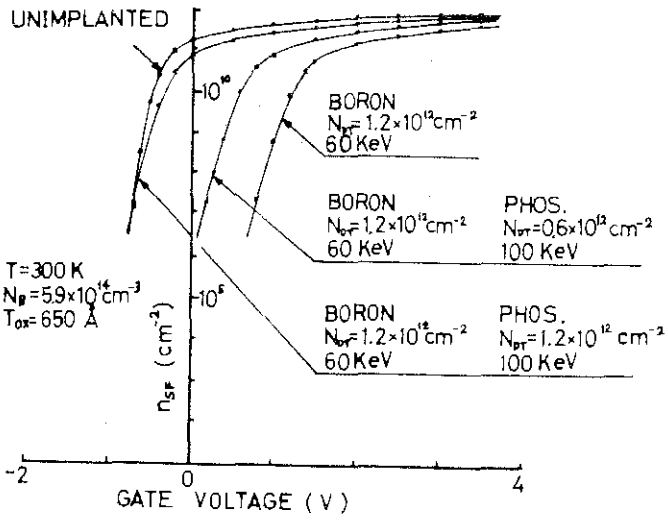


Figure 3.33 Experimental results of log n_{SF}-V_G curves for the condition shown in Fig. 3.31.

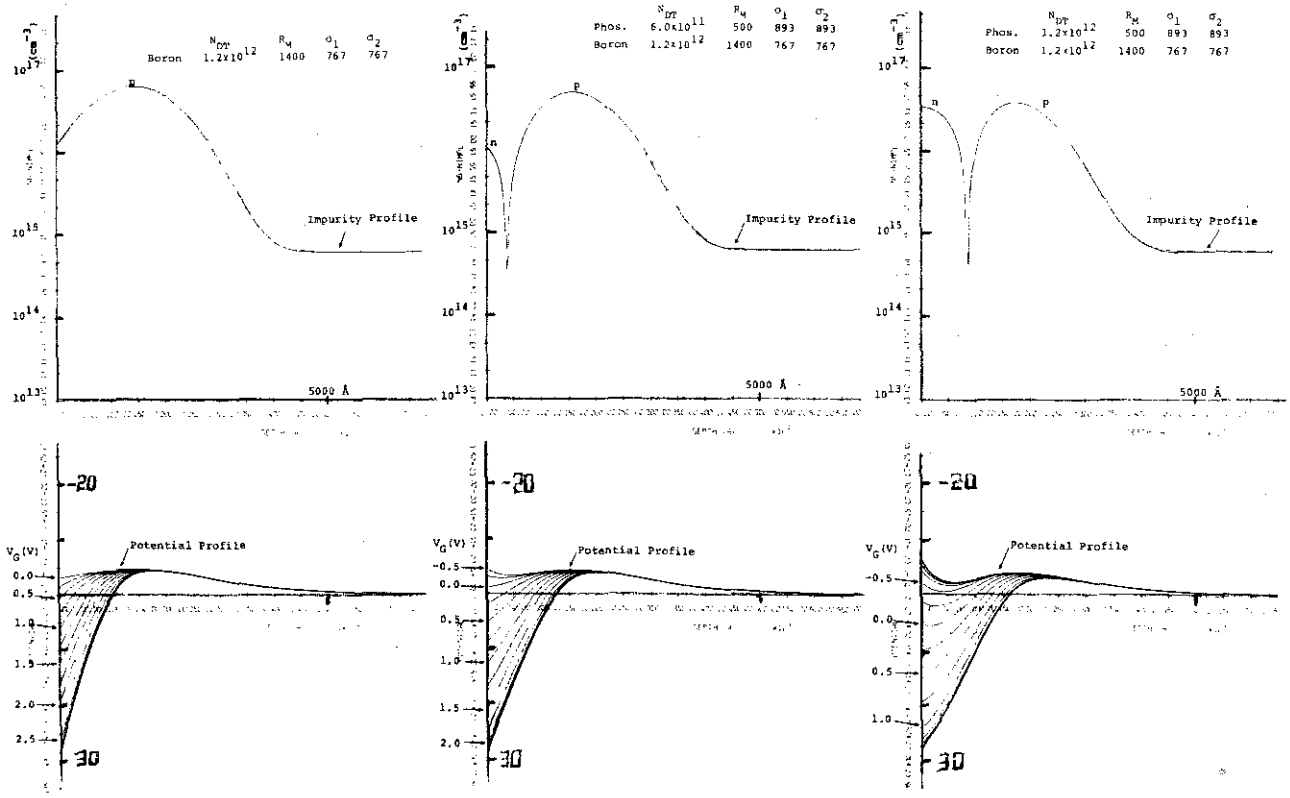


Figure 3.32 Potential profiles corresponding to the case shown in Fig. 3.31.

In Fig. 3.32, it is seen that the depletion layer is shielded by the boron layer for these implantation conditions. Thus this is equivalent to have a highly doped p-type substrate. The slope of log $n_{SF} - V_G$ curves in weak inversion region is, therefore, correspondingly decreased as shown in Fig. 3.31. The threshold voltage can be independently controlled by the n-type impurity at the surface. This means that the control of the slope of log $n_{SF} - V_G$ curves without threshold shift is even possible. Figure 3.33 illustrates the result of the measurements for MOSFET fabricated corresponding to the theoretical prediction shown in Fig. 3.31. The correlation seems satisfactory.

In general, the maximum value of the slope of log $n_{SF} - V_G$ curves is determined by the doping of the substrate because compensation for the substrate doping is extremely difficult. The double layer implantation only realizes less steep curves in comparison to the unimplanted case.

3.4.6 Conclusion

Low-level currents in MOS transistors with single and double layer implanted impurities have been discussed. A single boron layer in n-channel transistor causes positive threshold shift, however, the slope of log $I_D - V_G$ curve in weak inversion region tends to become less steep than that of unimplanted MOS transistor. On the other hand, a single phosphorus layer or arsenic layer in n-channel MOS transistor causes negative threshold shift, but residual current occurs. These features should be carefully considered in designing the threshold shift by ion-implantation.

The double layer implantation of opposite type impurities makes possible a control of these low level currents. Some of the examples discussed in this section are:

(1) Parallel shift of the log $I_D - V_G$ (log $n_{SF} - V_G$) curves both for enhancement and depletion mode transistors.

(2) Transistors with residual currents for load devices that feature in quasi-static operation of a flip-flop cell.

(3) Transistors that have less steep log $n_{SF} - V_G$ curves than unimplanted transistors.

Control of the low-level currents will be of special importance in the design of a low threshold dynamic memory circuit and a CMOS circuit. In view of this, the present analysis will provide a theoretical basis for determining appropriate ion-implantation conditions.

3.5 Double-Diffused MOSFET Analysis

3.5.1 Introduction

Double-diffused MOSFET (DMOSFET) was first proposed by H. Sigg [54] , and Y. Tarui et al. [55] The DMOSFET differs from the conventional device in that a p-type channel region having a higher doping than the substrate is formed by succesive diffusions of boron and phosphorus or arsenic. The second n-type diffusion makes n^+ source and drain regions and at the same time, determines the length of the channel region. The channel region has, therefore, a gradient of doping, whereas the region adjacent to the drain, the drift region, has a flat doping. Thus, originally the DMOSFET has asymmetrical structure about its midpoint. Symmetrical MOSFET having double-diffused regions both at the source and at the drain, is also useful device in memory applications in that bilateral switching is needed. An application of the symmetrical DMOSFET to a simplified CMOS device will be discussed in Chapter 5.

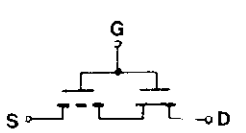
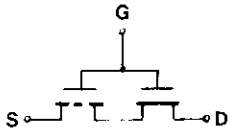
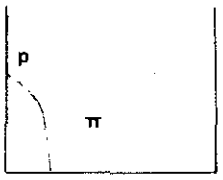
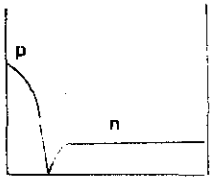
A significant advantage of the DMOSFET is that it realizes effectively short channel device without tight mask tolerances. This means that the switching speed of the device is fast. This has already been demonstrated in several prototype integrated circuits. [56], [57] Recently, Ohta et al. have fabricated an integrated logic circuit having a gate delay of 2 ns. [58] A high frequency DMOSFET having an f_T of 2 GHz has also been reported. [54] Since the power-delay product basically stays constant for a fixed circuit configuration and power supply voltage, this feature can be utilized for reducing the power dissipation of integrated circuits.

In this chapter, an analysis of DMOSFET is dealt with. The simplest way to analyze the DMOSFET is to express the device as a series connection of enhancement and depletion regions. This approach coincides with an analysis of E/D gate (Enhancement/

Depletion gate) MOSFET done by Masuda et al. [59] T. J. Rodgers et al. applied the E/D theory to analyze the DMOSFET, in which they modified the theory by taking velocity saturation of carriers and substrate bulk charge effect into account. [60] Numerical analyses of the p-p^- type DMOSFET were reported by Lin et al. [61] and by Sekigawa et al. [62] These analyses used varying levels of approximation, but their accuracies have not been entirely satisfactory.

The purpose of this chapter is to present a more precise numerical analysis of the DMOSFET in order to give a physical insight into the operation of DMOSFET. The analysis is made in such a way that will make possible to analyze several different DMOS structures. These include both the symmetrical (p-n-p and p-p^--p type) and asymmetrical (p-n and p-p^- type) DMOSFETs. An accurate form of mobility as functions of the drain field, the gate field and the doping is considered in analyzing the device. A brief comparison of the existing theories and the present analysis is illustrated in Table 3.4.

Table 3.4 Comparison of the existing DMOS analyses and the present analysis.

CIRCUIT ORIENT		DEVICE ORIENT	
H. MASUDA T. MASUHARA et al.	T.J. RODGERS S. ASAI et al.	H.C. LIN W. JONES	PRESENT WORK
			 p-n p-p^- p-n-p p-p^--p
CONSTANT MOBILITY	VELOCITY SATURATION INCLUDED	CONSTANT MOBILITY	MOBILITY $\mu(E_x, E_y, N_B)$
NO BULK CHARGE	WITH BULK CHARGE	$Q_N(y)$	$Q_N(y)$ EXACT POTENTIAL

3.5.2 Charge and Current Equations of DMOSFET

A three-section model of a typical p-n type asymmetrical DMOSFET is shown in Fig. 3.34. The device is divided into p-type channel region, n-type drift region and drain region. In each region, the concentration of charge is approximated as described in the following.

(1) P-type channel region

The charge equation for the free electron charge density Q_N is approximated in a manner similar to that described in Eqs.(3.24) to (3.26) in Section 3.3. Total surface charge Q_{SF}, bulk charge Q_B and electron charge Q_N are given by the following equations as functions of surface potential U_{SF}, Fermi potential U_F and quasi-Fermi potential ξ,

$$Q_{SF} = -C_D\left(\frac{kT}{q}\right)\left[e^{U_{SF}-\xi-U_F} + U_{SF}e^{U_F}\right]^{\frac{1}{2}} \qquad (3.52)$$

$$Q_B = -C_D\left(\frac{kT}{q}\right)\left[U_{SF}e^{U_F}\right]^{\frac{1}{2}} \qquad (3.53)$$

$$Q_N = Q_{SF} - Q_B, \qquad (3.54)$$

where C_D is Debye capacitance.

The surface potential U_{SF} is given by solving the equation relating the gate voltage U_G to the surface potential and quasi-Fermi potential as seen by

$$U_G = U_{SF} + \gamma\left[e^{U_{SF}-\xi-U_F} + U_{SF}e^{U_F}\right]^{\frac{1}{2}}. \qquad (3.55)$$

In order to express the variation of doping along the channel,

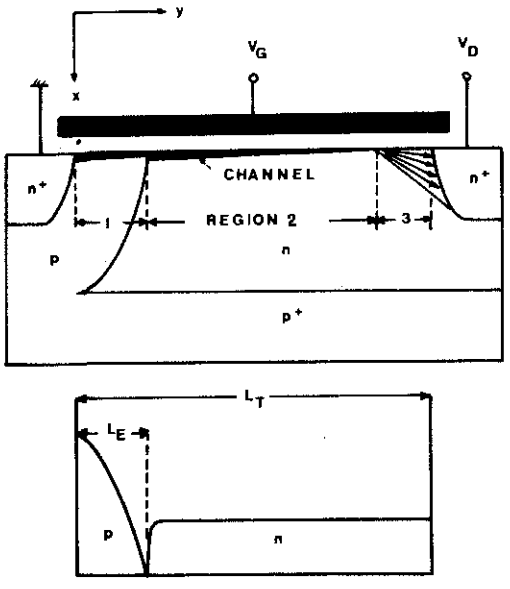


Figure 3.34 A three-section model of DMOSFET.

Fermi potential $U_F = \ln (N_A - N_D) / n_i$ is assumed to be a function of position. Strictly this is not correct because U_F is originally defined in the substrate and the variation of doping gives rise to a variation of built-in potential. This assumption is equivalent to express the entire transistor as a series connection of many separate transistor sections having different dopings.

(2) N-type drift region --- region 2

The basic equation (3.16) was modified assuming negative U_F and zero bulk charge Q_B. Electron charge Q_N is given by the equation,

$$Q_N = Q_{SF} = - C_D \left(\frac{kT}{q}\right) \left[e^{U_{SF} - \xi - U_F} \right]^{\frac{1}{2}} \qquad (3.56)$$

where U_{SF} is given by the solution of the equation,

$$U_G = U_{SF} + \gamma \left[e^{U_{SF} - \xi - U_F} - U_{SF} e^{-U_F} \right]^{\frac{1}{2}} \qquad (3.57)$$

In some cases this region has p-type doping. In such cases Eqs.(3.52) to (3.55) are continually used for this region.

In Eqs. (3.55) and (3.57), U_G is an effective gate voltage. This is calculated taking the effect of surface state density N_{ss} and the spacial variation of work function difference ϕ_{MS}, as seen by the equation,

$$U_G = \left(V_G - \phi_{MS} + \frac{qN_{ss}}{C_{OX}} \right) \left(\frac{q}{kT} \right) \qquad (3.58)$$

$$\phi_{MS} = \phi_M - \left(\chi + \frac{E_g}{2} + \phi_F \right) \qquad (3.59)$$

(3) Current equation in regions 1 and 2

The numerical calculation in regions 1 and 2 was done in the following manner. First, at the source quasi-Fermi potential and source voltage was set to zero. Corresponding charges Q_{SF}, Q_B and Q_N were determined from the Equations (3.52) to (3.54). The values of quasi-Fermi potential at subsequent points were calculated from the current equation,

$$\frac{d\phi}{dy} = \frac{I_D}{\mu Q_N W (kT/q)} , \qquad (3.60)$$

where μ is effective mobility of electrons and W is the width of the channel. Equation (3.60) results from applying the "gradual channel approximation" and therefore is valid only when the surface field E_x is considerably larger than the drain field E_y. Accordingly, the analysis continually checks on the indicated sizes of E_y and E_x in the regions 1 and 2. When E_y becomes greater than E_x, the analysis considers that the high-field drain region has been reached and the program continues the analysis using equations appropriate to region 3.

(4) Current equation in region 3

In region 3, the carriers are assumed to be injected away from the surface in an approximately triangular configuration as shown in Fig. 3.35.[34] The equations used for analysis in this region are:

$$\frac{d^2U}{dy^2} = -\frac{q}{kT}\frac{1}{\epsilon_S}\left(q N_A + \frac{J}{v}\right) \qquad (3.61)$$

$$J = I_D/(W x_s) \qquad (3.62)$$

$$x_s = \frac{x_D - x_C}{L_T}(y - y_{PO}) + x_C \qquad (3.63)$$

where v is carrier velocity, and other parameters are illustrated in Fig. 3.35.

The program performs numerical integration of quasi-Fermi potential using Eq. (3.60) in regions 1 and 2 and Eq. (3.61) in region 3 for a given current. The final value

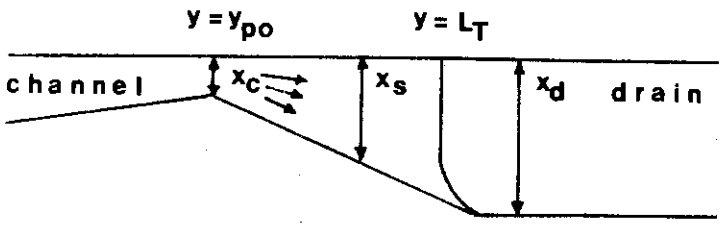


Figure 3.35 The approximation of the triangular space charge region near the drain in DMOSFET.

of quasi-Fermi potential at the drain gives the corresponding potential at the drain diffusion. In this integration 200 points were used.

(5) Mobility of electrons

Mobility of carriers is a function of the gate field E_x, the drain field E_y and the total doping N. However, as far as the author knows, there have been no complete theory taking these into account accurately. Therefore a semi-empirical form of mobility is used in the present analysis, as seen by the equations,

$$\mu = \mu_0 \left[1 + (\mu_0 E_y / v_{sat})^{\alpha} \right]^{-1/\alpha} \qquad (3.64)$$

$$\mu_0 = \mu_{max} \left[r + \frac{1 - r}{1 + 0.76\, N/N_r} \right] \left[1 + \theta E_x \right]^{-1} \qquad (3.65)$$

$$r = \mu_{min} / \mu_{max} = 0.1 , \qquad (3.66)$$

where $\alpha = 2$ for electrons, and $\alpha = 1$ for holes, $N_r = 6.3 \times 10^{16}$ cm^{-3}, saturation velocity $v_{sat} = 0.9 \times 10^5$ m/s and $\theta = 1.68 \times 10^{-8}$ m/V. The dependence upon doping given by Eq. (3.65) and the drain field dependence given by Eq. (3.64) are using the same form for bulk silicon. [63], [24] The gate field dependence given by Eq. (3.65) is obtained through careful comparison of the current-voltage curves between the numerical analysis and the experiments for samples listed in Table 3.2. The velocity field relationship for several conditions are illustrated in Fig. 3.36.

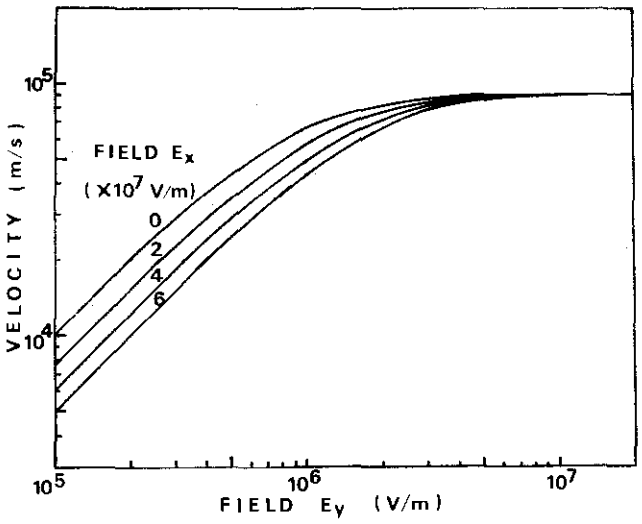


Figure 3.36 Drain field (E_y) dependence of mobility with gate field (E_x) as a parameter. Low field mobility of 1000 cm^2/V.s is assumed.

3.5.3 Results of the Analysis and the Comparison with Measurements

One of the purposes of this study is to compare the dc-current behavior and the potential profiles in various DMOSFET structures. The doping profiles that are analyzed through this analysis are shown in Fig. 3.37. A typical structure for discrete transistors for high frequency application is p-n type asymmetrical structure. For integrated circuit applications, it is common to use p^- or π type substrate to facilitate isolation between transistors without additional processing steps. Therefore the structures for transistors are either p-p^- type or p-p^--p type. The p-p^- type device is used as a driver transistor in inverter, and p-p^--p type device is used for dynamic memory circuit, in which bi-lateral switching action is needed to charge and discharge the memory capacitor. Another interesting application of the symmetrical structure is n-channel transistor in p-well of complementary MOS circuit. This will be discussed in Chapter 5.

(1) Analysis of standard MOSFET

Before going into discussions on double-diffused structures, let us first examine the results of the analysis for standard MOSFET. The reason for this is that the current-voltage behavior is well understood and through the comparison of the results with experiments the accuracy of the present analysis technique is verified.

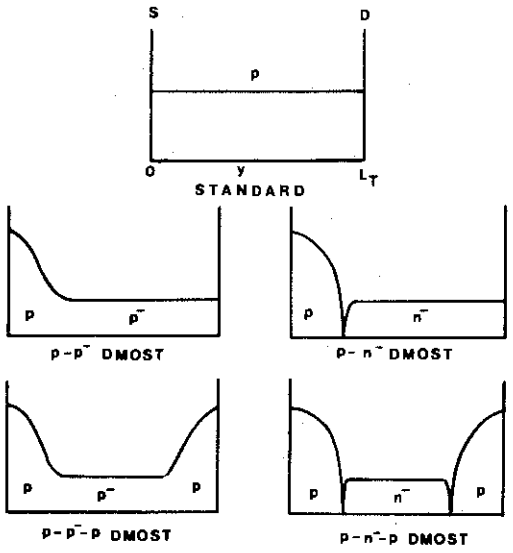


Figure 3.37 Various DMOSFET structures analyzed through this study.

Figure 3.38 shows $(I_D)^{\frac{1}{2}}$ vs. V_G curves in the saturation region for long channel devices having channel lengths of 20 and 50 microns. Three samples having gate oxide thicknesses of 220 Å, 600 Å and 1470 Å were used in order to demonstrate the agreement of the theoretical calculation with experiments over a wide range of gate field E_x. Calculated curve assuming a constant mobility is shown for the sample having 1470 Å gate oxide thickness. These samples are the same ones as have been used in Section 3.3.

Although drain field did not have significant influence in the above comparison, this should be considered in short channel cases. Figure 3.39 illustrates the calculation of potential profiles and mobility variations along the channel for MOSFETs having various channel lengths. For long channel case, the mobility is low at the source end of the channel and increases slightly toward the drain. This is entirely due to the variation of the gate field. However, in short channel device, the mobility is a decreasing function toward the drain, and in the region adjacent to the drain the carrier velocity saturates. This indicates that the drain field gives rise to a significant effect on the device behavior.

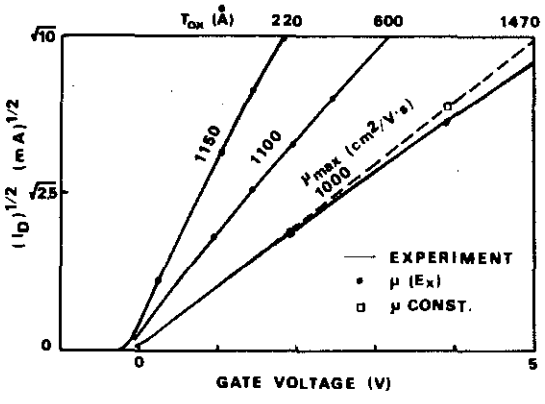


Figure 3.38 Comparison between the theory and experiments of $(I_D)^{\frac{1}{2}}$ versus V_G curves for conventional MOSFETs having gate oxide thickness of 220 to 1470 Å. The channel lengths for these samples are either 20 or 50 μm.

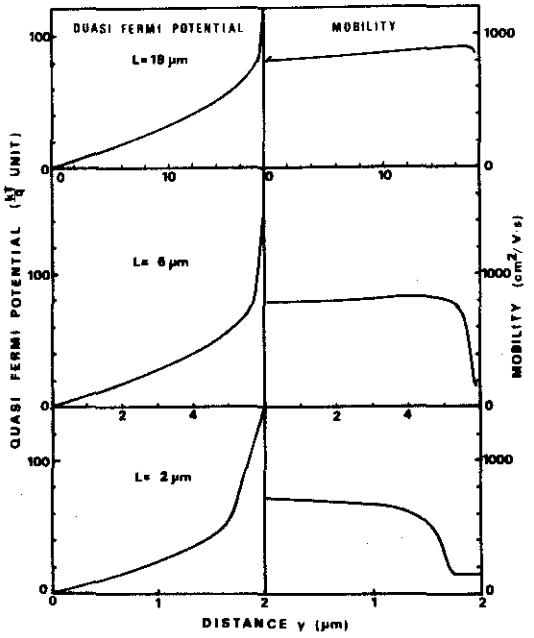


Figure 3.39 Quasi-Fermi potential and mobility varitions along the channel in standard MOSFETs.

One of the remarkable feature in the current-voltage relationship of the short channel device is that the saturation of the drain current occurs at a lower drain voltage than that expected by the constant mobility theory. In Fig. 3.40, calculated drain current vs. drain voltage curves for samples having the same aspect ratio W/L but different channel lengths are shown. It is seen that in the short channel case the value of the saturation drain current is about 60 to 70 percent of those in long channel devices, that is caused by the lower saturation voltage due to velocity saturation. Thus, the shape of the velocity-field curve affects on the shape of the corresponding current - voltage relationship near and beyond the saturation drain voltage significantly.

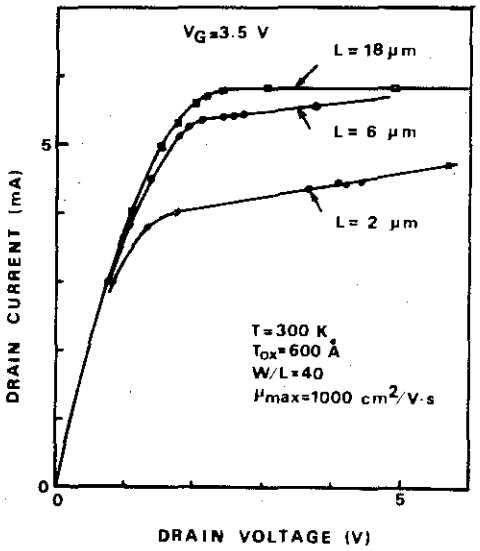


Figure 3.40 Calculated I_D versus V_D curves for standard MOSFETs having various channel lengths. W/L is equal for each case.

(2) Analysis of Double-Diffused MOSFET

In standard MOSFET, the current is inversely proportional to the channel length as far as the device is operated in the region where the carrier velocity does not saturate. This is not the case in the double-diffused MOSFET.

Figures 3.41 to 3.43 illustrate the calculated drain current vs. drain voltage curves for p-n type asymmetrical DMOSFET having various total channel lengths L_T. The length of the enhancement-type channel region is kept constant. The drain current at the saturation drain voltage is shown as a function of the gate voltage for these structures in Fig. 3.44. From these figures, the following features of the current-voltage relationship of the DMOSFET are

pointed out.

(1) The drain current in the saturation region is not inversely proportional to the total channel length. Especially, when the gate voltage is low, it is almost constant with the variation of the total channel length. This indicates that the current is controlled by the enhancement-type channel region L_E.

(2) The on-resistance, however, is inversely proportional to the total channel length L_T. Thus shorter channel length is desirable for applications that require low on-resistance. For example, the driver transistor in an inverter circuit needs low on-resistance because the on-level is determined by the ratio of the on-resistance of the driver and equivalent resistance of the load.

Let us discuss the effect of the doping profile on the device behavior in detail. The variation of the quasi-Fermi potential and mobility along the channel is shown in Figs. 3.45 to 3.47. These correspond to the structures shown in Fig. 3.41 to 3.43. It is seen that in any biasing conditions or device doping profiles, high field regions are observed at the source end and the drain end of the channel. Correspondingly, mobility dips are seen there. The first high field region, at the source end, has never been seen in standard MOSFET. This is due to the high concentration of doping and the corresponding high threshold voltage. The length of this high field region does not correspond to the length of the p-type channel region. For instance, in the device shown in Fig. 3.47, that has only p-type region but has a gradient of doping, the high field region is seen. This indicates that the simple two-transistor models illustrated previously, for instance, those of Masuda et al. [59] and Rodgers et al. [60] , need careful determination of the device parameters in dividing the device into two regions.

A comparison of the calculated current voltage curves with measurements was performed on a p-n type asymmetrical sample having a total channel length of 4 μm as shown in Fig. 3.48. It is seen that the agreement is good in the non-saturation region. However,

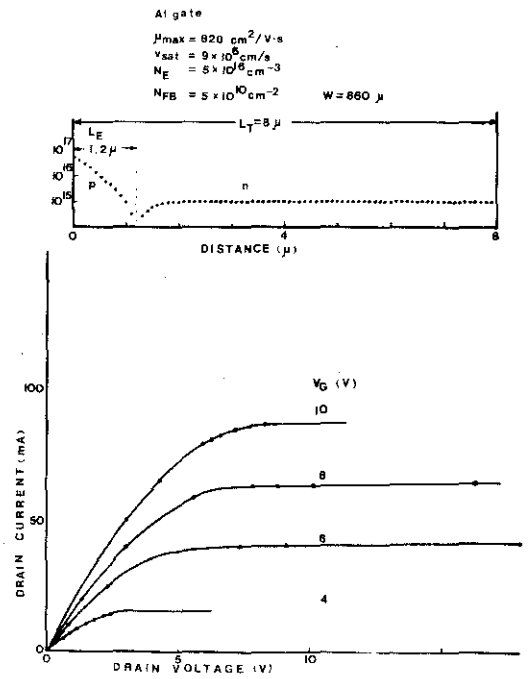


Figure 3.41 Drain current versus drain voltage curves for p-n type asymmetrical DMOSFET having L_T=8μm.

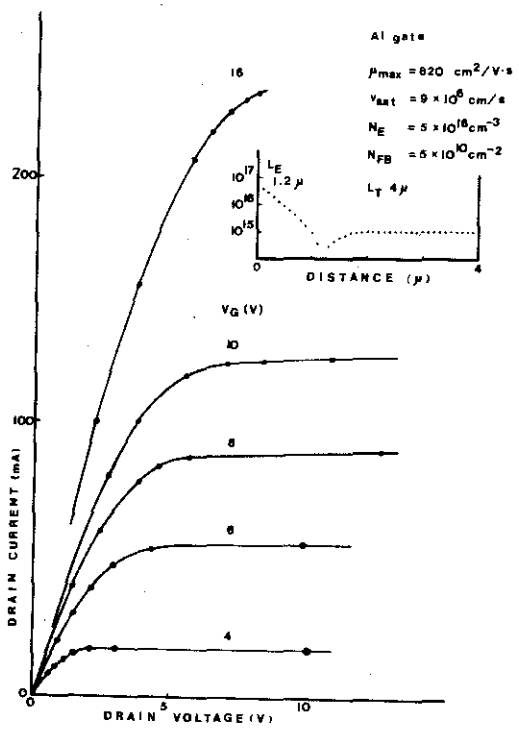


Figure 3.42 Drain current versus drain voltage curves for p-n type asymmetrical DMOSFET having L_T=4μm.

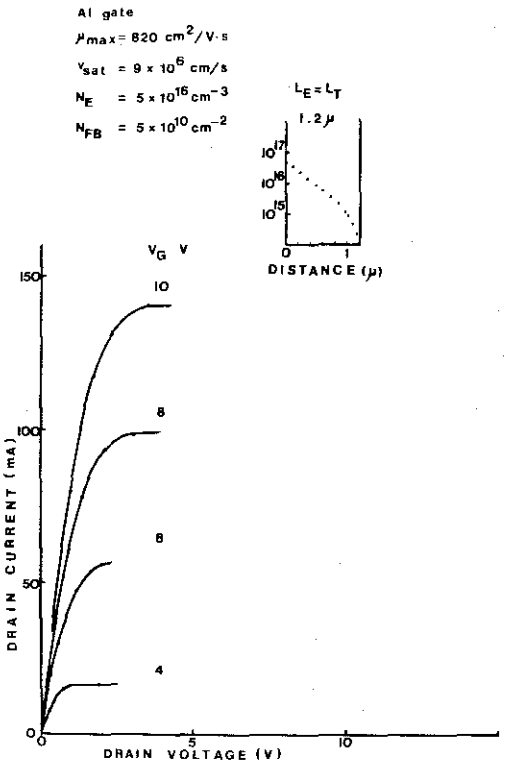


Figure 3.43 Drain current versus drain voltage curves for p-n type asymmetrical DMOSFET having L_T=1.2μm.

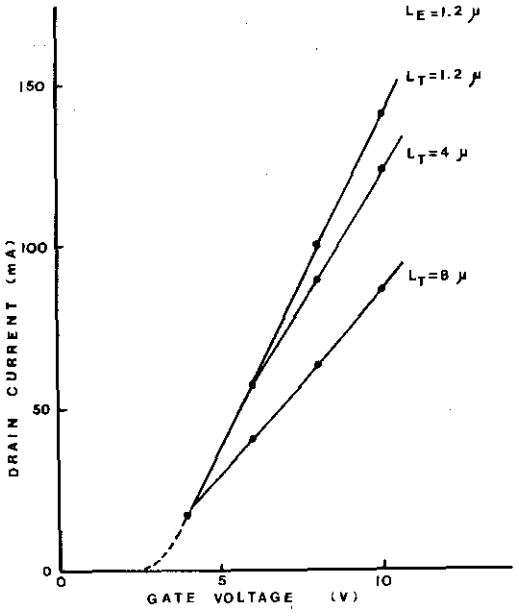


Figure 3.44 Drain current at saturation drain voltage versus gate voltage curves for p-n type asymmetrical DMOSFET having various total channel lengths but the same length for the p-region.

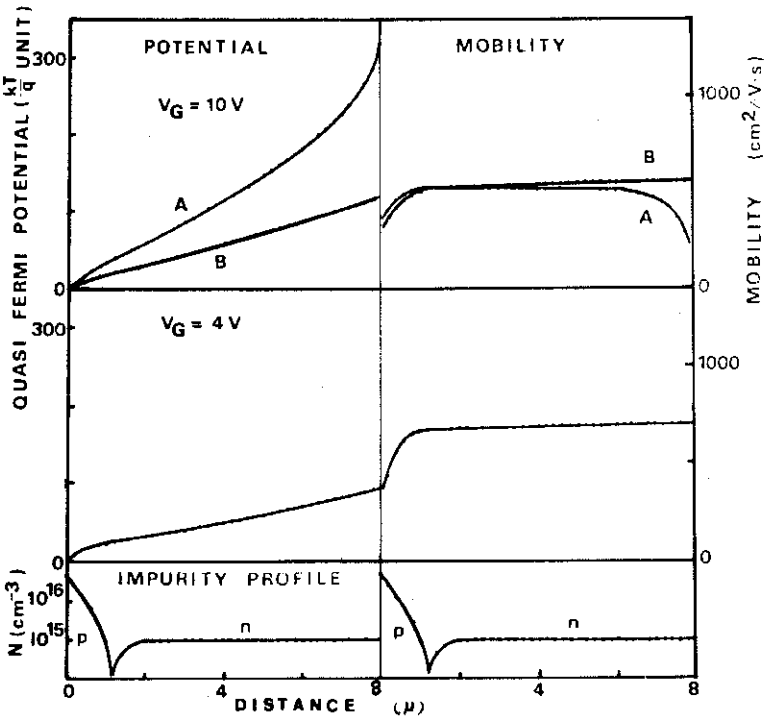


Figure 3.45 Quasi-Fermi potential and mobility variations along the channel in p-n type DMOSFET having $L_T=8\mu m$.

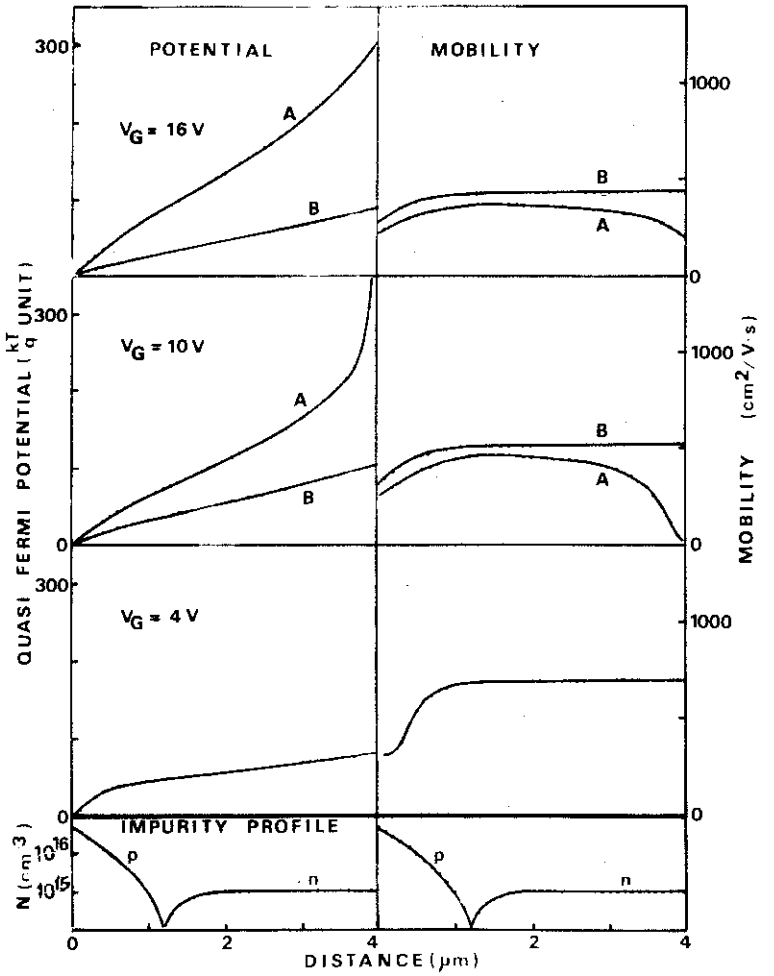


Figure 3.46 Quasi-Fermi potential and mobility variations along the channel in p-n type DMOSFET having $L_T=4\mu m$.

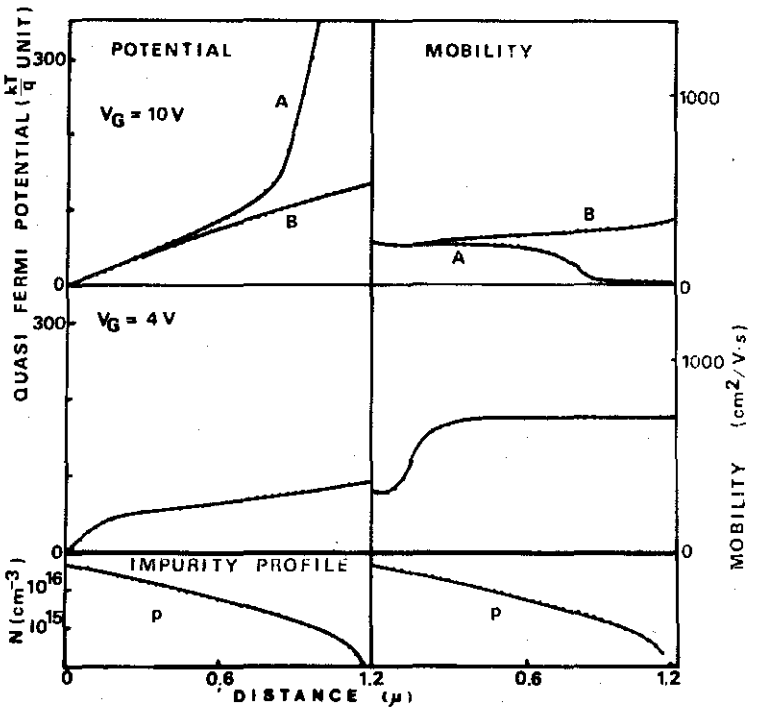


Figure 3.47 Quasi-Fermi potential and mobility variations along the channel in p-n type DMOSFET having L_T=1.2μm.

deviation is seen in the saturation region. In order to obtain a better fitting of the theoretical calculation to the measurements, several factors should be considered. First, precise measurements of the channel lengths for both the total channel and enhancement-type channel region, should be performed. At the same time doping profiles have to be measured accurately at the surface. The mobility expressions used in the present analysis are empirical ones, and no verification was done at high drain field. This measurement is difficult because it is almost impossible to bias MOS transistors with a uniform high drain field. Through this analysis it was observed that by varying the saturation velocity and the shape of the velocity-field relationship near the saturation velocity, the saturation voltage and the saturation current vary correspondingly. Therefore, further study is needed on this point. We, thus, conclude that for design purpose the accuracy of the present analysis is good.

We have discussed the current vs. voltage curves and potential distributions of p-n type asymmetrical DMOSFET. P-p^- type asymmetrical DMOSFET exhibits similar behavior because the only difference exists in the fact that the threshold voltage in the drift region is lower in p-n type device than in p-p^- type device. This gives rise to smaller saturation current in p-p^- type device. The comparison has been done by Rodgers et al. in Ref. [60], and is not repeated here.

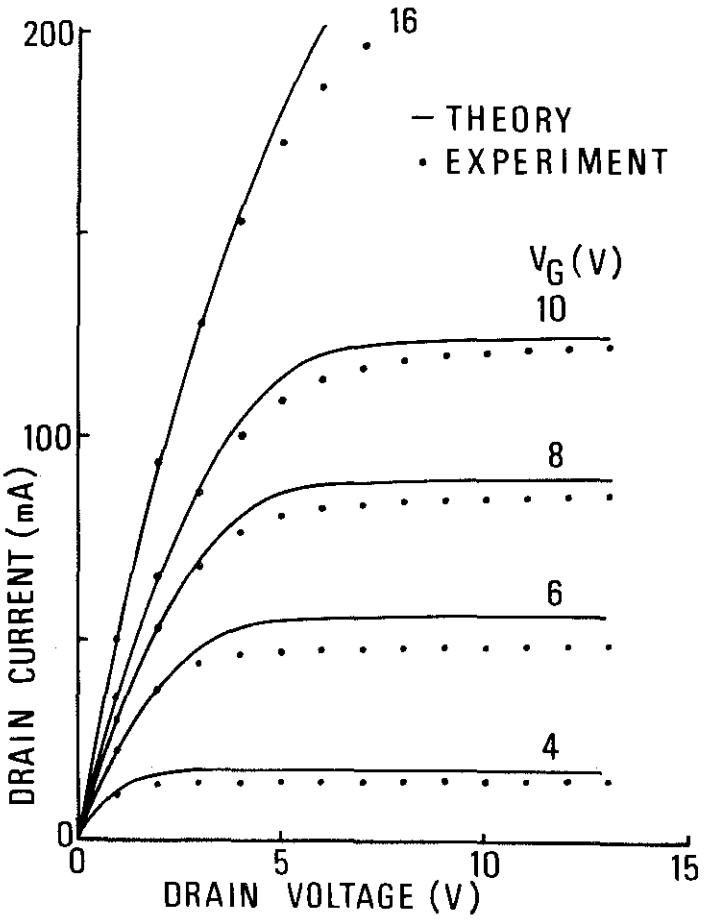
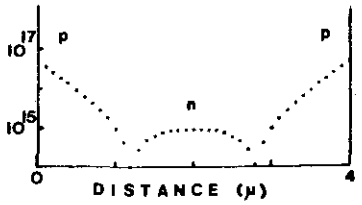


Figure 3.48 Comparison of the theory with measurements of drain current versus drain voltage curves for p-n type DMOSFET having $L_T=4\mu m$.

Symmetrical DMOSFET is an important structure in memory applications because bi-lateral switching action is inevitable in dynamic memory. This also has advantage in fabrication. In asymmetrical DMOSFETs, a masking step is needed when p-type channel region is implanted. However, in short channel device, this masking step is very critical because the mask has to be aligned within a tolerance of $L_T / 2$. In symmetrical DMOSFET, this alignment is avoided because it is not necessary to distinguish the drain and the source windows in implanting the p-type impurity for the channel region.

An example of the calculated current-voltage relationships for the symmetrical DMOSFET is shown for p-n-p type structure in Fig. 3.49. This device has the same parameters as the asymmetrical device shown in Fig. 3.42, except that the symmetrical device has a p-region adjacent to the drain. From the comparison of the two figures, it is seen that the saturation drain voltage is lower for the symmetrical device. This is because the saturation drain voltage is determined by the doping type and concentration near the drain. This results in a lower saturation current in the symmetrical device. For instance, it is 70 percent of that of the asymmetrical device at $V_G = 10$ V, and 60 percent at $V_G = 8$ V. It is expected that the breakdown voltage for the symmetrical device is lower than that of asymmetrical device because considerably high concentration of the fie-



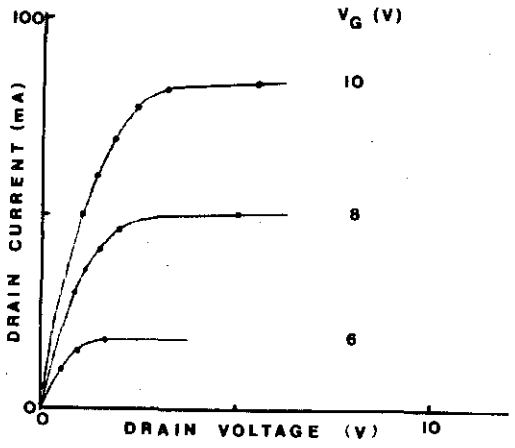


Figure 3.49 Calculated drain current versus drain voltage curves for a p-n-p type symmetrical DMOSFET having $L_T = 4\mu$m.

ld is observed near the drain due to the high doping. This, however, can be avoided if the p-type channel region is designed to be short so that the drain depletion layer would extend beyond the high doped region.

Another application of the symmetrical DMOSFET is n-channel device in CMOS integrated circuit. The DMOSFET in this case is formed through p-well diffusion through the source and drain windows followed by the n^+ diffusion. The p-well diffusion is performed in such a way that would make possible that p-regions from the source window and from the drain window touch and form a merged p-well. The corresponding doping profile is $p\text{-}p^-\text{-}p$ type symmetrical profile. Detailed discussion on the current-voltage relationships, potential profiles of the device and the comparison with the measurements will be presented in Sections 5.2 and 5.3.

3.5.4 Conclusion

A precise analysis of the double-diffused MOSFET was presented. The analysis is based on a three-section model of the DMOSFET. The following second-order effects are included in this analysis; (1) the diffusion current component, (2) exact calculation of the surface potentials and the corresponding induced electron number, (3) mobility variation due to the gate field, drain field and doping, (4) variation of the work function difference along the channel. The analysis can be applied to various double-diffused MOSFET structures, both symmetrical and asymmetrical.

Comparison of the dc-current behavior, quasi-Fermi potential distribution and mobility variation along the channel between the double-diffused MOSFET and standard MOSFET was made. It was found that a high field region exists at the source end of the channel in the double-diffused MOSFET. The theoretical calculation of the current-voltage curves was in good agreement with measurements in the non-saturation region. However, slight deviation was seen in the saturation region. For practical purposes, the analysis gives

good prediction of the current behavior with a short computer time.

The double-diffused MOSFET has a number of advantages over conventional MOSFET as a short channel device; (1) the threshold is insensitive to the shrinking of the channel length, (2) high punch-through breakdown voltage, (3) relatively deep drain junction and thick oxide allowed to obtain the same short channel effect as conventional device. These in turn mean that the one-dimensional analysis could be effective in a short channel devices that is not the case in conventional MOSFET. The present analysis, therefore, provides a good design tool in designing future integrated circuits utilizing double-diffused MOSFET.

3.6 Conclusion

This chapter presented accurate analyses for the dc-behavior of various types of MOS transistors. The conventional MOSFET, the ion-implanted MOSFETs and the double-diffused MOSFETs were analyzed.

A precise model for MOSFET having uniformly-doped substrate was first presented with an emphasis on subthreshold low-current region. The expressions for the drain current that cover the entire operating region of MOSFET, the subthreshold or the tail-current region, the saturation and the non-saturation regions, were derived. These equations were proved to have excellent agreement with the measurements. This indicates that exact calculation of the surface potentials utilized in the present theory is quite effective in order to obtain accurate approximation of the current near and below threshold voltage.

A numerical analysis of the log $I_D - V_G$ or log $n_{SF} - V_G$ relationship and of potential in the surface space charge region was made for ion-implanted MOSFET. The basic limitations of the threshold shift technique by a single-layer implantation, occurences of less steep tail current in boron implanted MOSFET and residual current in phosphorus implanted MOSFET, were solved by the double-layer implantation.

A numerical analysis of the double-diffused MOSFET that has a doping profile toward the source-to-drain direction, was performed. The analysis is based on basically the same accurate charge approximations used for the analysis of low-current region in the standard MOSFET in Section 3.3, but care was taken with varying doping profiles and high field effects. Fairly good agreement of the current versus voltage relationships was observed between the theory and measurements.

These models and analyses will provide theoretical basis in designing the transistors for low-voltage and low-power applications.

CHAPTER 4 DESIGN AND EXPERIMENTS OF DEPLETION LOAD (ENHANCEMENT/DEPLETION - E/D) CIRCUITS

4.1 Introduction

The discussion in Chapter 2 revealed that the enhancement/depletion (E/D) configuration makes possible an operation at lower voltage than that needed for the enhancement/enhancement (E/E) configuration, and has a potential advantage for low power circuits. Although the CMOS gives a very low power at low frequency operation, it suffers from a very complex process and low circuit density. For the E/D configuration the process can be much simpler, and the density of the circuit is even higher than E/E configuration. This results in a higher yield and a producability of larger chip sizes. These features have enabled a very wide use of the E/D configuration for medium power, five-volt, TTL compatible LSIs. The p-channel version [1], has extensively been manufactured, and the emphasis now is on the development of the n-channel version for microprocessors and memories.

There are several methods to manufacture the n-channel E/D circuits. These are; (1) Use of Al_2O_3 and Si_3N_4 for the shift of the threshold voltage, [2], [3], [4] (2) Use of the double-diffused MOSFET, [5] and (3) Ion-implantation for the channel region. [6]

In this chapter, a general design approach that can be applied to any of the existing processes for the E/D inverter configuration, will be given in Section 4.2. Since the largest problem in designing the integrated circuit is that the circuit should be operated with sufficiently large noise margins, the design approach is based on this viewpoint. The switching performances and the power also will be discussed over a wide range of the operating voltage, from five down to 1.5 volts.

The measured results will be shown for a single NOR gate and a 2048-bit read-only memory in the rest of the section. These

integrated circuits were realized by making use of a newly developed n-channel structure that consists of both enhancement mode MOSFET having a gate insulator of SiO_2 / Al_2O_3 double layer and depletion mode MOSFET having a gate insulator of SiO_2 / phosphosilicate glass double layer.

Application of the E/D configuration to the peripheral circuits of random-access memories will be discussed in Section 4.3. A dynamic operation of E/D circuit is proposed. The measured performance of the prototype RAM array will be compared with the calculation by a circuit analysis program.

4.2 N-Channel Logic Using E/D Static Circuit [7]

4.2.1 Design Considerations of E/D Inverters

A. Device Equations

For the purpose of simplifying the design, the simplest current equations of Hofstein model are employed. In each region, these are given by

(1) Cutoff region $V_G - V_S \leqq V_T$

$$I = 0. \tag{4.1}$$

(2) Saturation region $0 < V_G - V_S - V_T \leqq V_D - V_S$

$$I = (\beta/2)(V_G - V_S - V_T)^2. \tag{4.2}$$

(3) Nonsaturation region $V_D - V_S \leqq V_G - V_S - V_T$

$$I = \beta[(V_G - V_S - V_T)(V_D - V_S) - \tfrac{1}{2}(V_D - V_S)^2], \tag{4.3}$$

in which,

$$\beta = \frac{W}{L}\frac{\epsilon_{ox}}{T_{ox}}\mu \qquad (4.4)$$

where V_D, V_S and V_G are drain, source and gate voltages, and V_T denotes the threshold voltage. Although the term "pinch-off voltage" is commonly used for depletion mode MOSFET, "threshold voltage" is used for both MOSFETs in this chapter.

The threshold voltage is modulated by positively biasing the source terminal. This body effect is especially important for the load MOSFET because its source-to-body voltage is significantly varied in actual use. The modulated threshold is given by

$$V_T = V_T(V_S = 0) + K[(V_S + 2\phi_F)^{1/2} - (2\phi_F)^{1/2}] \ , \qquad (4.5)$$

in which Φ_F is Fermi potential, and K is the constant given by

$$K = (T_{ox}/\epsilon_{ox})\ (2q\epsilon_S N)^{1/2} \qquad (4.6)$$

B. Static Characteristics

The E/D configuration described here is shown in Fig. 4.1. The circuit has dc-transfer curves as the one shown in Fig. 4.2 schematically. Several characteristic voltages representing the

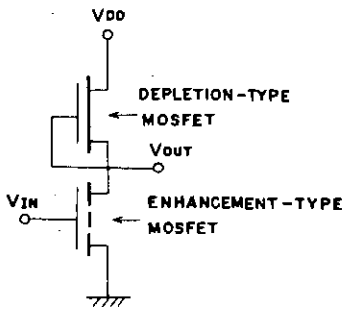


Figure 4.1 Inverter circuit with a depletion type load.

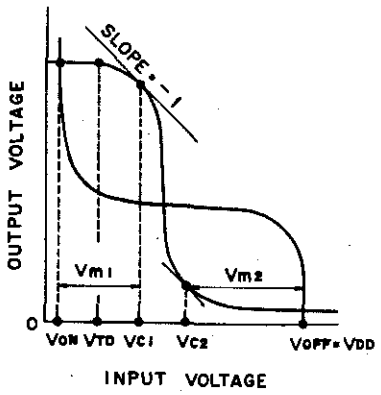


Figure 4.2 Schematic dc-transfer characteristics of the inverter with a depletion-type load MOSFET.

shape of the transfer curve are also shown in Fig. 4.2. When the enhancement driver transistor is off, depletion load transistor is conductive, and apparently, off-level V_{OFF} that is equal to the supply voltage appears at the output node.

$$V_{OFF} = V_{DD}. \tag{4.7}$$

Other circuit parameters, on-level V_{ON} and circuit threshold V_{c1} and V_{c2} are approximated by using Eqs. (4.2) and (4.3) for the driver and the load depending on the operation regions, and seen as,

$$V_{ON} \simeq V_{TL}^2 / \left[2(V_{DD} - V_{TD}) \beta_R \right] \tag{4.8}$$

$$V_{c1} \simeq - V_{TL} / \left[\beta_R (1 + \beta_R) \right]^{\frac{1}{2}} + V_{TD} \tag{4.9}$$

$$V_{c2} \simeq -\left[2 / (3\beta_R)^{\frac{1}{2}} \right] V_{TL} + V_{TD} \tag{4.10}$$

$$V_{m1} = V_{c1} - V_{ON} \tag{4.11}$$

$$V_{m2} = V_{OFF} - V_{c2} . \tag{4.12}$$

In these equations, subscripts "D" and "L" mean the parameter for the driver and the load MOS transistors. It should be noted that Eq. (4.7) applies only when the load transistor is operated in depletion mode region. This means that V_{TL} is negative when a back bias voltage of V_{DD} is applied, and that is the usual case. Equations (4.8) and (4.10) are derived assuming that the driver transistor is in the nonsaturation region and the load transistor is in the saturation region. Equation (4.9) is derived in an opposite manner. Care should be taken, therefore, when the inverter does not show normal dc-transfer curves. In such cases the assumptions are not true and these Equations are not valid.

The largest noise margin is obtained when the inverter switches at $V_{IN} = \frac{1}{2} V_{DD}$. This condition is expressed by using the cir-

cuit threshold voltages V_{c1} and V_{c2} as seen by the equation,

$$V_{c1} + V_{c2} = V_{DD}. \tag{4.13}$$

From Eqs. (4.9), (4.10) and (4.13), the relationship between the two threshold voltages V_{TD} and V_{TL} to satisfy the largest noise margin condition is calculated, and is seen as,

$$2V_{TD} - \left\{ \frac{1}{[\beta_R (1+\beta_R)]^{\frac{1}{2}}} + \left(\frac{4}{3\beta_R} \right)^{\frac{1}{2}} \right\} V_{TL} = \frac{K[(V_{DD} + 2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}]}{[\beta_R (1+\beta_R)]^{\frac{1}{2}}} + V_{DD} . \tag{4.14}$$

Next, let us discuss a generalized design approach using dimensionless voltages. Eqs. (4.7) to (4.12) can be expressed by using dimensionless or normallized voltages v (= V / V_{DD}), as follows.

$$v_{off} = 1 \tag{4.15}$$

$$v_{on} = \frac{v_{tl}^2}{2\beta_R (1 - v_{td})} \tag{4.16}$$

$$v_{cl} = v_{td} - \frac{v_{tl}}{[\beta_R (1+\beta_R)]^{\frac{1}{2}}} \tag{4.17}$$

$$v_{c2} = v_{td} - \left(\frac{4}{3\beta_R} \right)^{\frac{1}{2}} v_{tl} \tag{4.18}$$

$$v_{ml} = v_{cl} - v_{on} \tag{4.19}$$

$$v_{m2} = 1 - v_{c2} \tag{4.20}$$

The effect of the threshold voltage modulation due to substrate bias is neglected in these equations. For largest noise margin condition, Eq. (4.14) is modified to the following form.

$$2V_{td} - \left\{ \frac{1}{[\beta_R (1+\beta_R)]^{\frac{1}{2}}} + \left(\frac{4}{3\beta_R} \right)^{\frac{1}{2}} \right\} V_{tl} = 1 \qquad (4.21)$$

Before going into detailed discussions on optimum design of the inverter, let us briefly examine the influences of the device parameters on the dc-transfer curves. Figure 4.3 (1) to (3) show the examples of the dc-transfer curves of the E/D inverter operated with 5-volt supply. These are calculated results based on Eqs. (4.1) to (4.6). The parameters are (1) substrate bias constant K, (2) driver/load transconductance ratio β_R, and (3) load threshold voltage V_{TL}. The features of the transfer curves seen in Fig. 4.3 are:

(1) Off-level is equal to the supply voltage.
(2) The circuit threshold is higher than the threshold voltage of the driver MOSFET.
(3) Both the geometries and the threshold voltages of MOSFETs can be adjusted to obtain large noise margins.
(4) The circuit threshold varies with the substrate bias constant K.

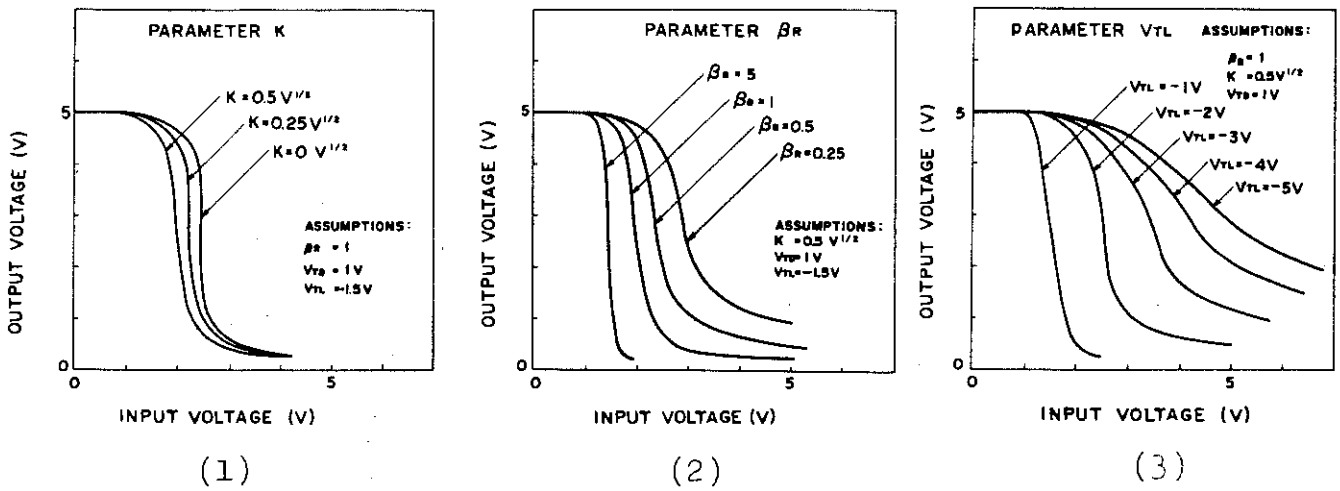


Figure 4.3 Calculated dc-transfer characteristics of the depletion-load inverter.

These features are expressed in the derived equations for the circuit voltages V_{c1}, V_{c2}, V_{OFF} and V_{ON} quantitatively.

Next, let us consider a generallized design approach of the inverter by using normallized voltages. We consider two design approaches;

(A) The case in that on-level is given as a specification.

(B) The case in that maximum noise margin is needed.

In CASE (A) , a set of design curves as shown in Fig. 4.4 are drawn on a v_{td} - v_{tl} plane that are calculated from Eq. (4.16). In the figure, the two circuit threshold voltages v_{c1} and v_{c2} are obtained. These are calculated from the following equations that are derived from Eqs. (4.16) to (4.18).

$$v_{td} = \frac{1}{\beta_s}(v_{c1}\beta_s - v_{on}) - [(v_{c1}\beta_s - v_{on})^2 - \beta_s (v_{c1}^2\beta_s - 2 v_{on})]^{\frac{1}{2}} \tag{4.22}$$

$$\beta_s = 1+\beta_R \tag{4.23}$$

$$v_{td} = \frac{1}{3} (3 v_{c2} - 4v_{on}) + [(3 v_{c2} - 4 v_{on})^2 - 3 (3 v_{c2}^2 - 8 v_{on})]^{\frac{1}{2}} \tag{4.24}$$

Let us show an example of how to use the figure. First, we assume that $v_{td} = 0.2$ and $v_{tl} = -0.4$, that is $V_{TD} = 1$ V, and $V_{TL} = -2$ V when the supply voltage is 5 volts. The figure indicates that $\beta_R = 1.1$ is appropriate for $v_{on} = 0.1$. The corresponding circuit threshold voltages are: $v_{c1} = 0.48$ and $v_{c2} = 0.66$. This means that this design is slightly off from the largest margin condition.

In CASE (B) , we calculate Eq. (4.21). The resulting curves for the relationships between v_{tl} and v_{td} are shown in Fig. 4.5. For convenience, constant v_{on} curves are also shown in the figure which are obtained from Eqs. (4.22) and (4.24). A design example shown in the figure indicates that when $v_{td} = 0.2$ and $v_{tl} = -0.3$ are assumed, $\beta_R = 0.85$ gives the largest noise margin. The corresponding $v_{on} = 0.066$.

The general design utilizing the normallized voltages described here is quite useful because one does not have to refer different design equations or design diagrams for different supply voltages. However, since the effect of the substrate bias is neglected, this causes error in calculating circuit threshold voltages. Especially, high level circuit threshold V_{cl} is strongly influenced by the substrate bias effect as shown in Fig. 4.3. This gives rise to an error in calculating noise margin V_{ml}. Consequently, this is a good approximation only when the value of K is small. This condition corresponds to the case in that a thin gate oxide and a low substrate are chosen.

The above discussion indicates that for more accurate design, separate design diagrams are needed depending on the specific supply voltages and device parameters determined. Two examples of the design diagrams for the largest noise margin condition are shown in Figs. 4.6 and 4.7 taking the supply voltages of

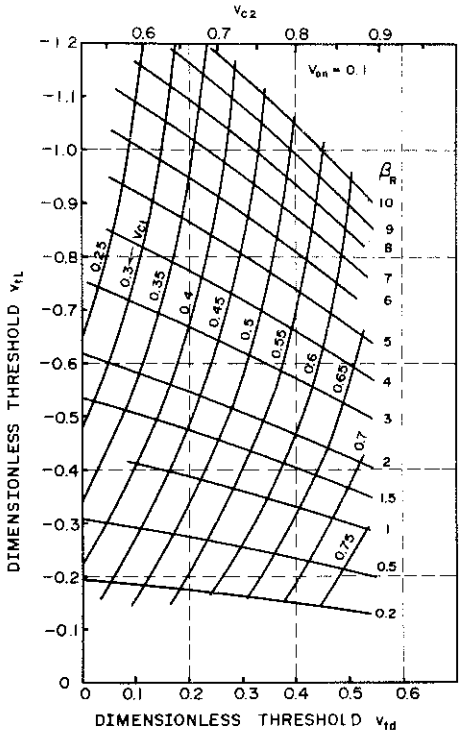


Figure 4.4 Relation between v_{tl}, v_{td} and β_R when $v_{on}=0.1$.

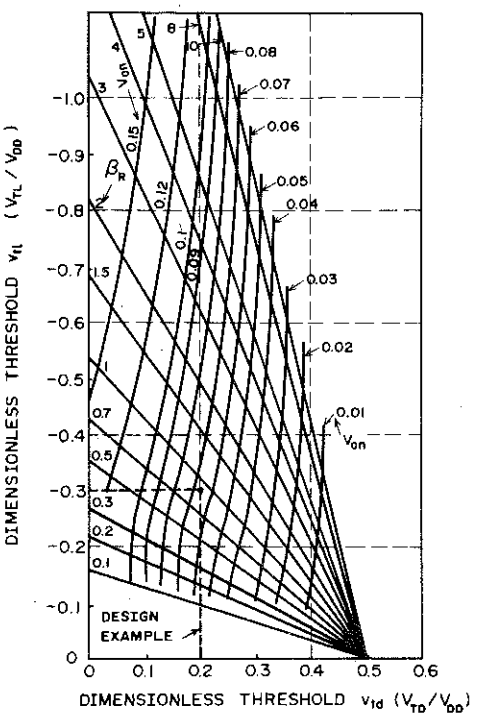


Figure 4.5 Relation between v_{tl}, v_{td} and β_R at maximum noise margin condition.

five and 1.5 volts. The difference between Fig. 4.5 and these figures can be seen when $|V_{TL}|$ is low. This is because the conductance of the load device is significantly modified due to the variation of the threshold voltage. When $|V_{TL}|$ is too low, the load transistor becomes enhancement mode if the source node is high level. To obtain a high level V_{OFF} equal to the supply voltage V_{DD}, this state should be avoided, and the load threshold $|V_{TL}|$ should be above a certain limit. This region is shown in Figs. 4.6 and 4.7.

Let us see the difference in designing optimum conductance ratio β_R at different supply voltages. We assume that $v_{td} = 0.2$ and $v_{tl} = -0.8$ are chosen. These correspond to $V_{TD} = 1$ V and $V_{TL} = -4$ V for $V_{DD} = 5$ V, and $V_{TD} = 0.3$ V and $V_{TL} = -1.2$ V for $V_{DD} = 1.5$ V. The optimum values of β_R are 4.5 from Fig. 4.5 (normallized voltage), 3.6 from Fig. 4.6 ($V_{DD} = 5$ V), and 4.0 from Fig. 4.7 ($V_{DD} = 1.5$ V). It is seen that at lower supply voltages, the effect of the substrate bias is not significant.

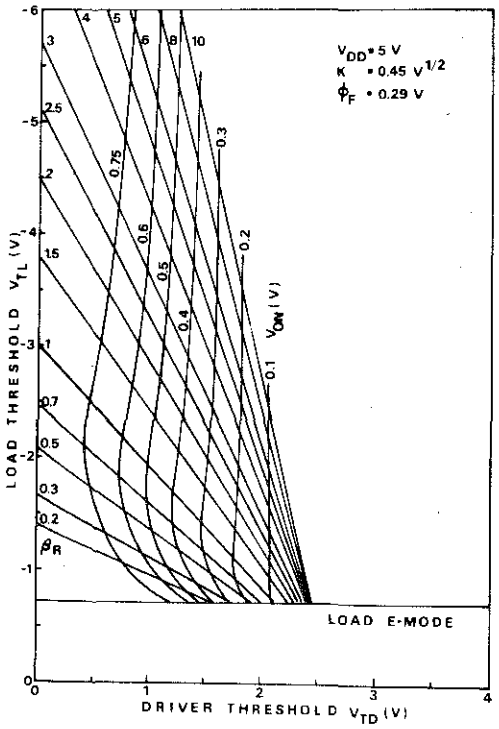


Figure 4.6 Design diagram to determine the thresholds and β_R for V_{DD} =5V.

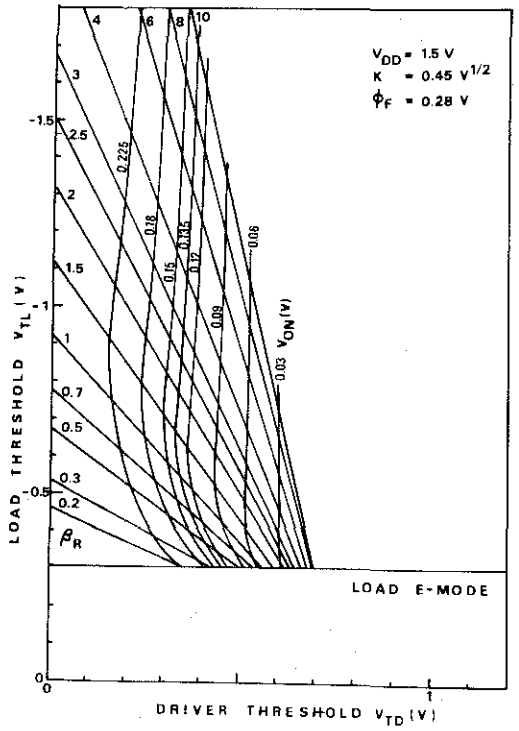


Figure 4.7 Design diagram to determine the thersholds and β_R for V_{DD} =1.5V.

The discussion so far has neglected the influence of the low-level currents described in Chapter 3. It is,however, noted that the optimum value of the threshold is relatively low for 1.5-volt operation. This indicates that considerations on the tail current in the driver MOSFET are needed for more precise design.

C. Transient Characteristics and Power-Delay Product

It is well known that in the enhancement-load inverter, the current through the load transistor is in proportion to V^2. In E/D configuration described here, the load transistor exhibits a nearly constant-current type current-voltage relationship. For this reason, the E/D configuration has a relatively high turn-off switching speed in compared with the enhancement-load circuit.

Let us make a brief comparison of the switching time between these circuits when the driver transistor turns off. The following assumptions are made in this comparison.

(1) Both circuits are operated with single power supplies, that is, V_{GG} for the enhancement-load and V_{DD} for the E/D configuration.
(2) Off-levels are equal for both circuits, thus, $V_{GG} = V_{DD} + V_T$.
(3) On-levels are equal for both circuits.
(4) The driver MOSFETs have the same channel geometries for both circuits.

In the E/D configuration, a time $t_{\frac{1}{2},D}$, defined as a time to charge up the voltage at the output node from the low level to a half of the supply voltage, is approximated by

$$t_{1/2,D} \simeq \frac{C}{\beta_{L,D} v_{tl}^2 V_{DD}} , \qquad (4.25)$$

in which C is the capacitance at the output node, and the substrate bias effect is neglected. In the case of the enhancement-load operated in the saturation region, $t_{\frac{1}{2},E}$ is given by

$$t_{1/2,E} \simeq \frac{2C}{\beta_{L,E}(V_{GG} - V_T)} . \qquad (4.26)$$

From the assumption (2), the ratio $t_{\frac{1}{2},E} / t_{\frac{1}{2},D}$ leads to

$$\frac{t_{1/2,E}}{t_{1/2,D}} \simeq 2v_{t1}^2 \left(\frac{\beta_{R,E}}{\beta_{R,D}}\right) , \qquad (4.27)$$

where driver/load conductance ratio β_R is used instead of β_L. Since the on-resistances of the driver MOSFETs are equal for both circuits, the load currents should be equal in order to satisfy the assumption (3). Thus, $V_{TL}^2 / \beta_{R,D} = V_{DD}^2 / \beta_{R,E}$. Substituting this relationship into Eq. (4.26), we have

$$\frac{t_{1/2,E}}{t_{1/2,D}} \simeq 2 \qquad (4.28)$$

It is seen that the shape of the load curve in the E/D inverter has resulted in approximately twice as fast switching speed as the case in the enhancement-load inverter. If a comparison is performed on the basis of equal power dissipation, the result will be more advantageous for the E/D configuration because the enhancement-load needs higher power supply.

In Fig. 4.8, the results of the detailed computer calculations of the turn-off characteristics of the E/D inverter are shown in that the effects of the three device parameters K, β_R and V_{TL} are

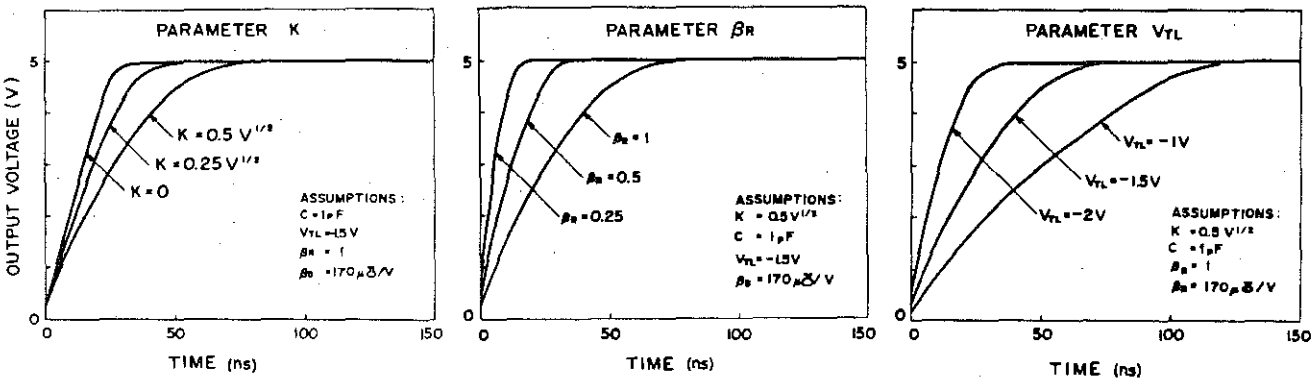


Figure 4.8 Calculated turn-off responses of the E/D inverter.

illustrated. It is seen that when the substrate bias constant K is large, the turn-off time becomes large. This is caused by the departure of the load curve from the constant-current type due to the substrate bias effect. Another remarkable feature of the turn-off transient is that the turn-off time is strongly dependent on the value of V_{TL}. This in turn means that the variation of V_{TL} leads to the variation of the switching speed. Therefore, the threshold of the load is again the important design parameter as it was the case in the dc-design of the E/D inverter.

Delay time per a stage in an inverter chain consisting of the inverters having the same design, gives a good estimation of the delay time in actual logic or memory circuits. Since the value of the parasitic capacitances between the stages strongly depends on the device and lithography, the capacitance was normalized to 1 pF. Thus the delay per picofarad as denoted by t_d/C (ns/pF) was calculated. Figures 4.9 and 4.10 show the delay at $V_{DD} = 5$ V and 1.5 V. On-levels are shown in the figure because it

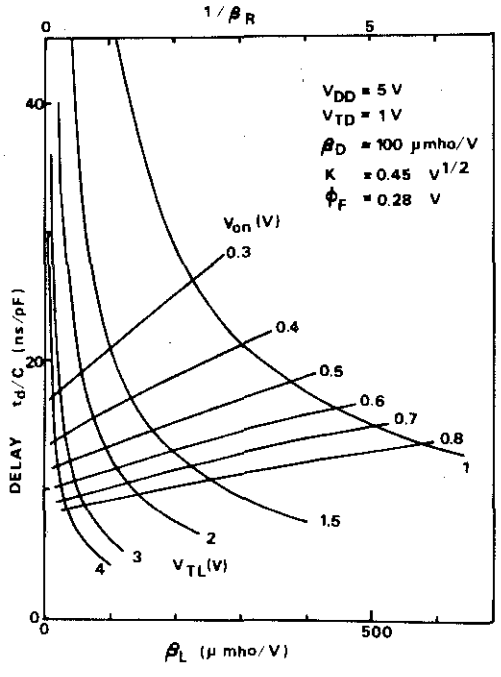


Figure 4.9 Delay time of the E/D inverter with a supply voltage of five volts.

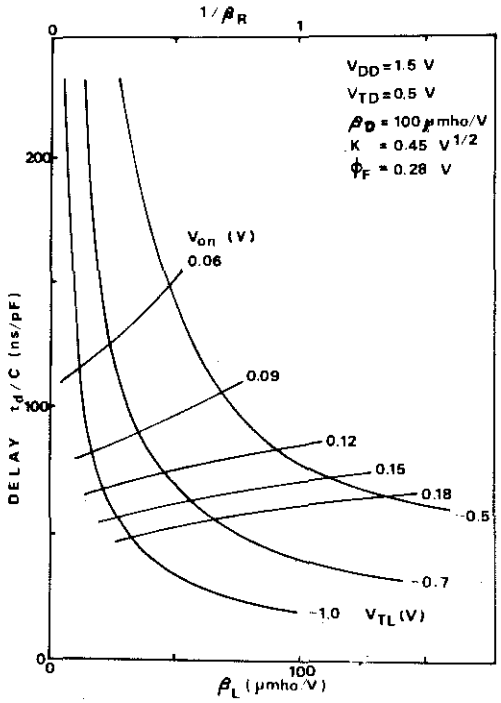


Figure 4.10 Delay time of the E/D inverter with a supply voltage of 1.5 volts.

is an important design parameter. These curves are for an inverter having a driver transistor whose channel conductance is 100 μ.mhc/V. Thus, if the driver transistor has conductance of 200 μ.mho/V, horizontal scale should be doubled and the vertical scale should be halved. It is seen from these figures that the delay at 1.5 volts is almost an order of magnitude larger than that at 5 volts.

Let us finally discuss power-delay product. Power dissipation when an inverter is "on" is given by

$$P_{ON} \simeq (\beta_L/2) V_{TL}^2 V_{DD}. \tag{4.29}$$

Therefore, the power increases in proportion to V_{DD} if we consider a specific circuit having a fixed design of β_R and V_{TL}. However, if we consider the case in that the parameters can be chosen at different supply voltages so that the inverter exhibits a good dc-transfer curves, we will see different aspects. For instance, if we assume that the dimensionless threshold voltages are kept constant at different supply voltages, Eq. (4.29) leads to,

$$P_{ON} \simeq (\beta_L/2) v_{tl}^2 V_{DD}^3 \tag{4.30}$$

This means that the power increases with V_{DD}^3 in such cases.

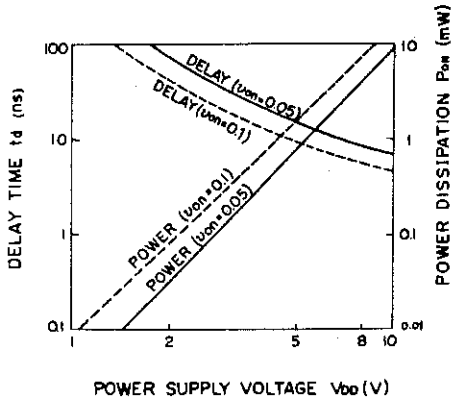


Figure 4.11 Calculated delay time and power dissipation as a function of supply voltage when $V_{TD}=1V$, $V_{TL}=-1.5V$, and $\beta_D=170\mu$.mho/V.

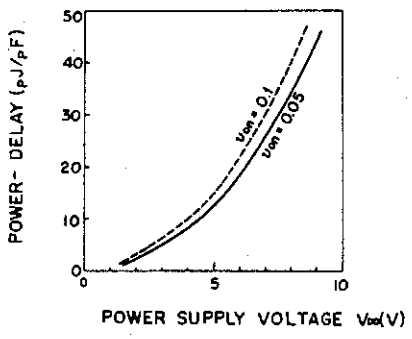


Figure 4.12 Power-delay product calculated from Fig. 4.11 as a function of supply voltage.

In a practical design, both V_{TL} and β_R are adjusted at different supply voltages. In this case, too, it is shown that the power increases with V_{DD}^3. Combining Eqs. (4.25) and (4.29), power delay product of the E/D inverter is expressed as

$$P_{ON} \times t_{1/2,D} \simeq (C/2)V_{DD}^2. \qquad (4.31)$$

Although Eq. (4.31) gives a rough estimation of the power-delay product, more accurate results are obtained from the inverter chain. Figures 4.11 and 4.12 show the power-delay product as a function of the supply voltage. It is seen that the power delay product is 10 to 15 pJ/pF at 5 V, and 1 to 1.5 pJ/pF at 1.5 V. It should be noted that the power-delay product is small when V_{ON} is small and β_R is large. This indicates that the delay caused by the driver transistor to discharge the capacitance, can not be neglected when β_R is small and the on-level is large. In order to obtain a smaller power-delay product, it is desirable to use as low supply voltage as possible. This, however, is limited by the minimum threshold voltages achievable without the variation for both enhancement and depletion devices.

4.2.2 Experimental Results

Some test circuit are designed based on the design considerations discussed in the previous section. These integrated circuits are fabricated by making use of a newly-developed n-channel technology. Figure 4.13 illustrates a cross-section of the integrated circuit. The substrate is 10 ohm.cm (100) p-type silicon. Enhancement MOSFET has an Al_2O_3 layer over thermally-grown SiO_2 as the gate insulator. The threshold voltage was controlled by varying the thickness ratio of the SiO_2/Al_2O_3 layer down to +1 volt[8] to operate the circuit with a single +5-volt supply voltage. The enhancement-type MOSFET has an electron mobility of about 1000 $cm^2/V.s$, that is about five times greater than that of conventional p-channel MOSFET. Depletion-type MOSFET has an SiO_2 layer passivated with PSG as a gate insulator, and the threshold is about -1.5 volts. At the isolation region, the field insulator of phosphosilicate glass over Al_2O_3 has a threshold of approximately 50 volts. Thus, each MOSFET is perfectly isolated. The details of the processing technology were reported by Hashimoto et al. [9], [10]

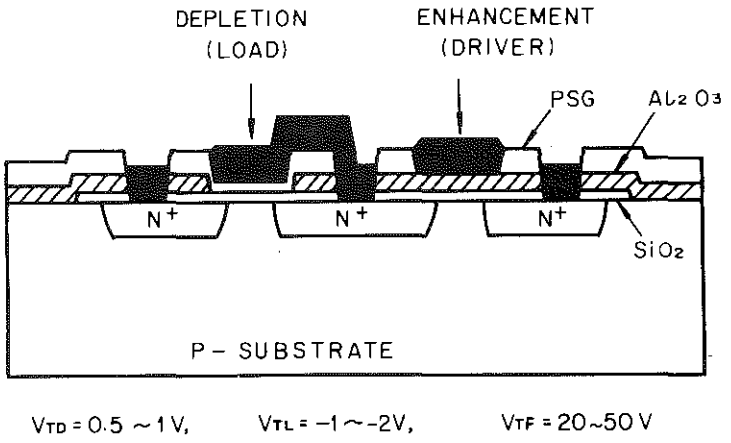


Figure 4.13 Cross section of the n-channel MOS integrated circuit.

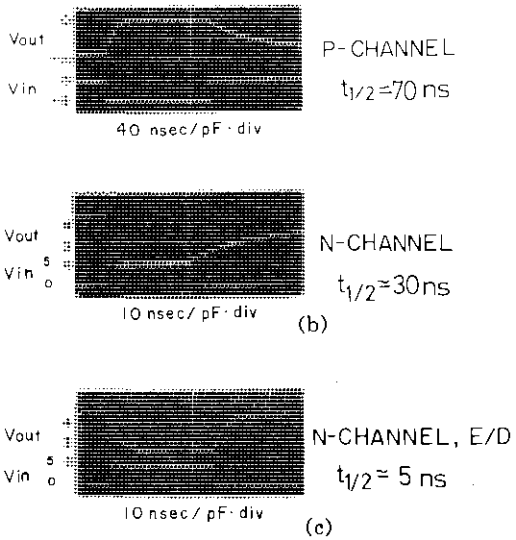


Figure 4.14 Comparisons of the switching speeds. (a) p-channel enhance-ment load(P_{ON} =1.6mW), (b) n-channel enhancement load (P_{ON}=0.9mW), (c) n-channel depletion-load inverter (P_{ON}=3.0mW) with the driver transistor of the same geometry.

Figure 4.14 shows the measured transient waveforms of a single NOR gate in compared with p-channel and n-channel enhancement load circuit with driver transistors having the same aspect ratios. It is seen that the n-channel E/D circuit exhibits almost an order of magnitude improvement in the switching speed over the p-channel enhancement-load circuit. The measured power-delay product was 15 pJ/pF at 5-volt supply and 6 pJ/pF at 3-volt supply for the E/D inverter. These are about twice better figures than those obtained for the n-channel enhancement-load inverter operated with the same supply voltages V_{DD}. These results correlate well with the calculations shown previously. The factors contributing to the reduction of the switching delay are summarized as follows.

(1) Reduction of the power-delay product by the use of the E/D configuration which is by a factor of two to three.
(2) High electron mobility of the n-channel device.
(3) Low threshold voltage obtained for the driver transistor.

The basic technology was applied to a large array. Figure 4.15 shows a 2048-bit read-only memory. The circuit schematic is

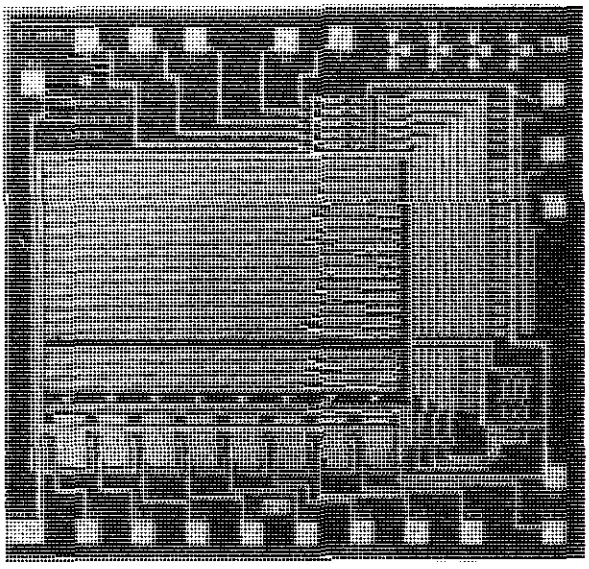


Figure 4.15 Entire MOSLSI chip of the 2048-bit read-only memory. Actual size of the chip is 3.2×3.0㎟.

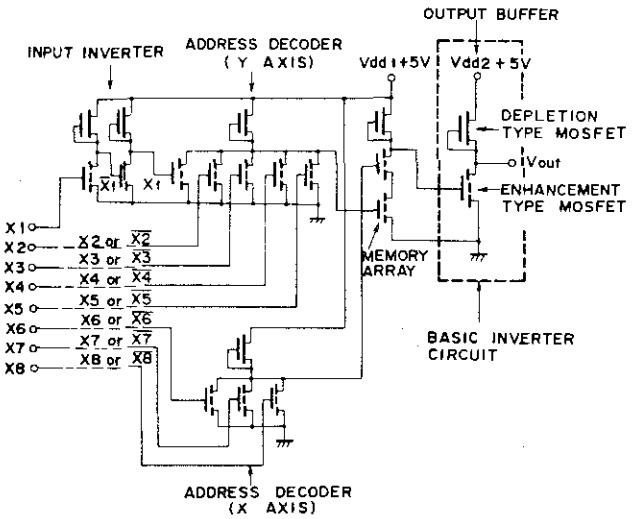


Figure 4.16 Circuit diagram of the 2048- bit n-channel read-only memory.

shown in Fig. 4.16. The array consists essentially of five-stage cascades of inverters, i.e., two input buffers, an address decoder, and an output buffer. Each stage has a depletion-load. For this reason, the circuit is a good example to demonstrate the feasibility of the technology and to apply the design theory discussed in this chapter.

Input-output dc-transfer curves of the read-only memory are shown in Fig. 4.17. The total circuit has a threshold of approximately 1.6 volts and a low-level of 0.2 volts that are independent on the supply voltage. The output buffer can sink a current of 3 mA when the low-level voltage is 0.4 volts. Therefore, the chip is fully TTL-compatible both at the input and the output. The measured output waveform of the chip is shown in Fig. 4.18 when a "1" location is read. Also shown here is the output waveform of the p-channel read-only memory having the same chip size and the same memory pattern. A speed advantage by a factor of seven is achieved.

Summarizing the features of the chip;

(1) 2048 bits (256 words by 8 bits) fully-decoded static read-only memory,
(2) 300-ns total access time,
(3) +5-volt single power supply, and TTL compatible,
(4) 100 mW total power dissipation.

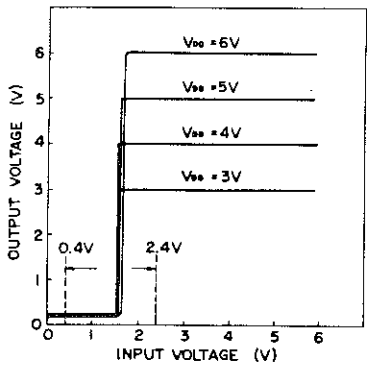


Figure 4.17 Measured dc-transfer characteristics of the read-only memory.

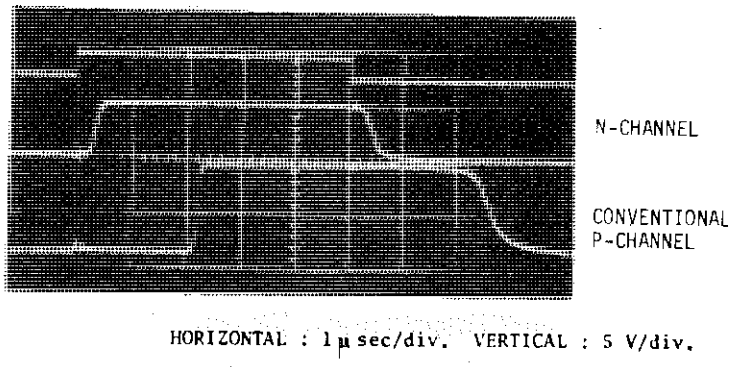


Figure 4.18 Measured output response of n-channel E/D type and conventional p-channel read-only memory. Input pulse is shown at the top.

4.3 N-Channel Random-Access Memory Using Dynamic E/D Circuit [11]

MOS integrated circuit memory has become the major technology for computer main memory. To reduce cost for a bit, increase of the cell number on a chip has bocome the general tendency in IC memories. This has so far been achieved by reducing the number of the transistors in memory cells. For instance, a classical cell used 6-MOS flip-flop. [12] The gradual advancement of the circuit technology enabled a 4-MOS cell [13], and a 3-MOS cell. [14]. Finally, a 1-MOS cell is now being used extensively. [15] Dynamic operation has been utilized in the cells having transistors less than four. In the dynamic cells, the memory charge is stored accross a capacitor that comprises basically of p-n junctions and a gate insulator. It appears therefore that the memory characteristics are quite sensitive to the leakage current. Typical operating voltages for these dynamic memories are 10 to 15 volts, and more than two supplies are now common. However, as pointed out in the previous section, single +5-volt operation is quite attractive from the system designer's viewpoint.

Several problems have to be solved if one wants to design dynamic memories operating at +5 volts.

(1) Low threshold enhancement-type MOSFET is needed for low voltage operation. The circuit therefore becomes sensitive to the low level tail current.
(2) Voltage loss in addressing circuits yields very low voltage stored at the memory cells.
(3) Delay time increases when the transistors are driven by low gate voltages.

This section discusses these problems associated with single +5-volt operation of dynamic memories. A new addressing circuit will be proposed that is utilizing a dynamic E/D configuration. This makes possible a fast access time at low voltage. The results of the computer circuit analysis made by a circuit analysis program HICAD [16], and the measured performance on a prototype RAM

will be discussed.

4.3.1 Problems in Designing Low-Voltage Dynamic Memories

We first consider what are the main problems in device design and circuit design of dynamic MOS memories operating at +5-volts.

Figure 4.19 illustrates schematically the circuit diagram for a 3-MOS and a 1-MOS type memory. The difference in these cell configurations exists in the method of reading. The 3-MOS type cell has a sense transistor Q_S in the cell, but the 1-MOS type cell does not. Thus in the 1-MOS type cell, charge stored across the capacitor C_M has to be transferred to the data line capacitance C_D for reading. The value of C_M usually is much smaller than C_D, and the signal voltage at the data line is comparatively small. This means that a special sense circuit having high sensitivity is needed in the 1-MOS type memory. On the other hand, the method of writing is the same for both memories. The charge across the data

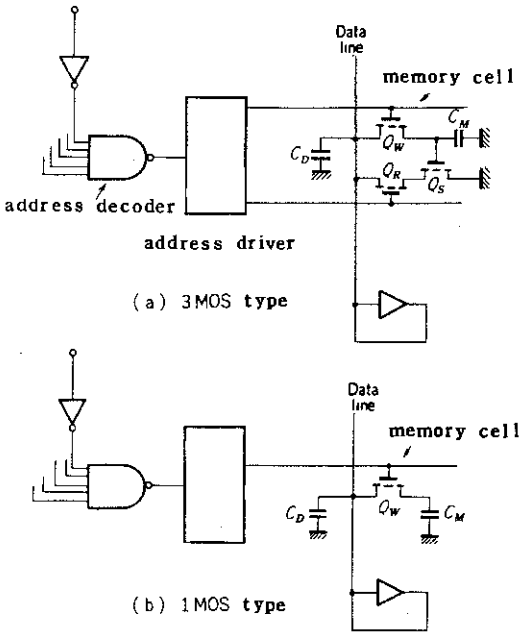


Figure 4.19 Schematic circuit diagrams for 3-MOS and 1-MOS type memory.

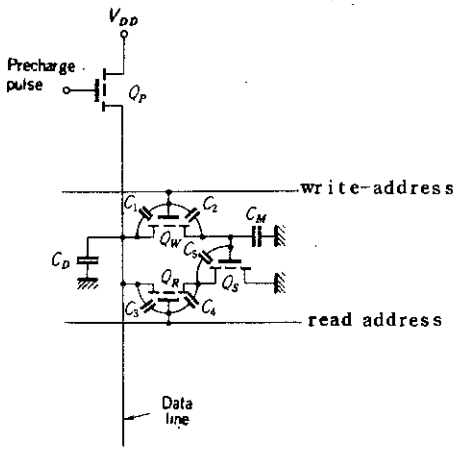


Figure 4.20 3-MOS type memory cell with parasitic capacitances.

line capacitance C_D is transferred to the memory cell. Thus, the problems associated with writing are common for both cells. In this section the 3-MOS type cell is mainly discussed.

The 3-MOS type memory cell and a precharge MOS transistor is shown in Fig. 4.20. Now, let us consider the voltage loss associated with writing. Figure 4.21 illustrates the results of the circuit analysis when "1" is written in the cell and then read. In the figure, precharge, write address and read address pulses have a high level of 5 volts. It is seen that a high level of approximately 2.5 volts is written in the cell. By varying the heights of these pulses and the supply voltage, high level voltage in the cell varies as shown in Fig. 4.22. The voltage loss arises from the feature of the source follower circuit. First, long time is needed for the precharge transistor to charge up the data line capacitance. Second, the high level voltage in the cell is limited by the gate voltage at the write transistor because a voltage loss of V_T can not be avoided in the source follower.

The above discussion suggests two effective approaches to achieve low voltage operation. First, low threshold voltage is required. Second, no voltage loss is allowed to drive the memory cells. Let us discuss these problems in the subsequent sections.

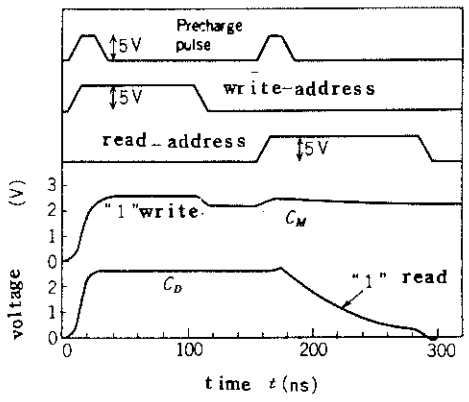


Figure 4.21 Waveforms for write "1", and read "1" in the cell. (Computer calculation)

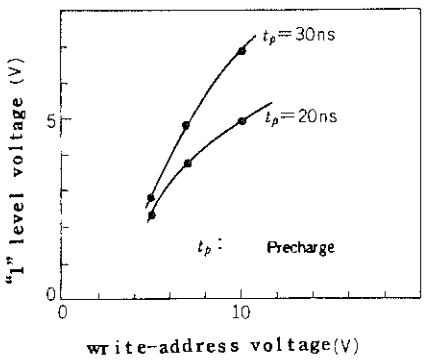


Figure 4.22 "1" level voltage in the memory cell versus write address voltage.

4.3.2 MOSFET Design Taking Tail Current into Account

Since low voltage operation needs low threshold voltage for MOSFET, care should be taken with subthreshold characteristics of MOSFET. Detailed discussions on the subthreshold characteristics of MOSFET have been made in Chapter 3 for both unimplanted and implanted cases. It was pointed out for most cases, the log I_D - V_G curves are approximated as straight lines whose slopes are functions of substrate doping, gate oxide thickness and ion-implantation condition. The important parameter is ΔV_G that represents the gate voltage variation corresponding to one order variation of the drain current.

A general design diagram for the threshold voltage is illustrated in Fig. 4.23. Since dynamic memories should guarantee a refresh time of more than 2 ms at 70°C, threshold characteristics at room temperature and at 70°C are drawn. The threshold voltage here is defined as the gate voltage when the drain current is 1 μA for convenience. We assume that the high level in the cell V_M "1" and the low level zero are distinguished at the voltage level of V_{MR}. We also assume that the time needed for the high level node

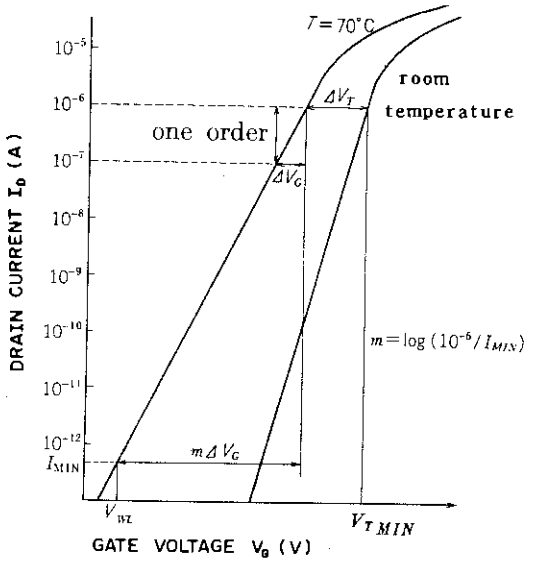


Figure 4.23 Determination of the threshold voltage taking the tail current of MOSFET into account.

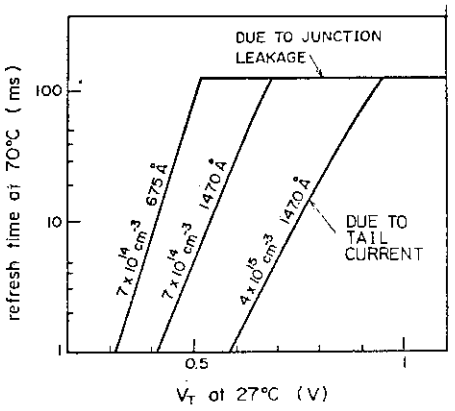


Figure 4.24 Storage time at 70℃ versus threshold voltage at room temperature.

to be discharged from V_{M}"1" to V_{MR} is t_{sMIN}. The corresponding current is given by

$$I_{MIN}=C_M(V_{M"1"}-V_{MR})/t_{s\,MIN}. \tag{4.32}$$

This is the maximum allowable current to obtain a storage time of more than t_{sMIN}. Let us now define a number "m" as denoting a logarithmic ratio of (current at the threshold / I_{MIN}).

$$m=\log(10^{-6}/I_{MIN}) \tag{4.33}$$

Gate voltage variation that corresponds to the preceding current ratio is m ΔV_G (70°C), where ΔV_G is the gate voltage variation corresponding to one order of current variation in the tail current region. We assume that the difference of the threshold voltage at room temperature and at 70°C is ΔV_T. This is calculated from the temperature dependence of the Fermi potential in Eq. (2.1). More accurate results of the temperature dependence of the threshold are obtained from the MOSFET model discussed in Section 3.3. The threshold voltage at room temperature should be designed so that the following relationship is fulfilled.

$$V_T > \Delta V_T + m\Delta V_G(70°C) + V_{WL} \tag{4.34}$$

Here, V_{WL} is the low-level voltage at the write-address line. The values for ΔV_G for various temperatures, substrate dopings and gate oxide thicknesses are obtained from Figs. 3.13 and 3.14 for unimplanted case. For implanted case, some results are shown in Section 3.4. Figure 4.24 shows examples of the dependence of the refresh time on several design parameters. If one needs a refresh time of more than 10 ms at 70°C, it is seen that the threshold voltage at room temperature should be above 0.42 volts for the device having a doping density of 7×10^{14} cm^{-3} and a gate oxide of 675 Å. For the device having a doping density of 4×10^{15} cm^{-3} and a gate oxide of 1470 Å, the required threshold voltage at room tempera-

ture is 0.75 volts. This indicates that the margin for the threshold is wider for the device having thin gate oxide and low substrate doping concentration. If ion-implantation of boron for n-channel device is done to shift the threshold voltage toward the positive direction, a special precaution is necessary because ΔV_G increases. Very shallow implantation or double-layer implantation of p and n-type impurities are two possible approaches to avoid the decrease of margin in threshold determination.

4.3.3 Address Circuitry in a Low-Voltage Dynamic RAM

A typical circuit that is used for address driver of dynamic memories is a bootstrap driver shown in Fig. 4.25. [17] The circuit works as follows. First, when the address is selected, the output node of the decoder goes high, and the capacitors C_{BS} and C_{BD} are charged through the transistor Q_{SW}. Then, write pulse is applied to the drain of Q_{DR}. Since Q_{DR} is ON, capacitor C_A is gradually charged. This in turn pulls up the gate voltage of Q_{DR} through the feedback capacitor C_{BS}. Thus the transistor Q_{DR} works as a constant current source that is similar to depletion mode device. Consequently, the voltage loss is eliminated. However,

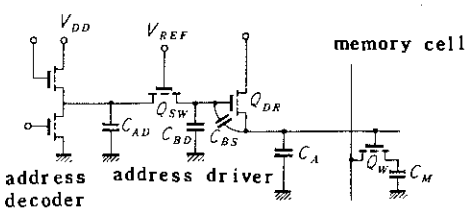


Figure 4.25 Conventional boot-strap address driver.

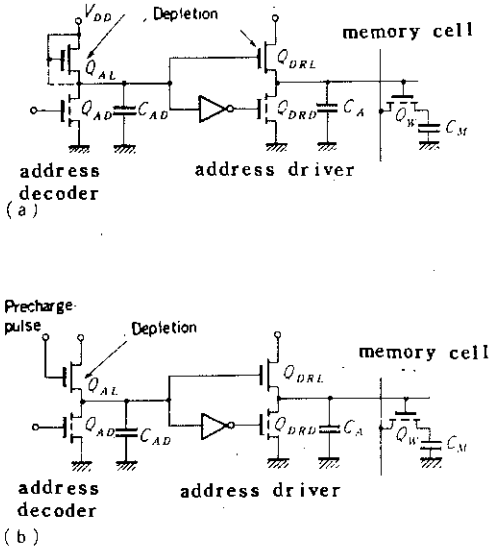


Figure 4.26 Proposed addressing circuits.

this circuit needs a high capacitance ratio C_{BS}/C_{BD} so that the bootstrap works effectively. This means that relatively large C_{BS} is required that occupies large area and the load capacitance for the previous stage becomes large.

In this section, two types of addressing circuit are proposed that utilize E/D configuration as illustrated in Fig. 4.26. These are:

(a) address decoder with static E/D circuit and push-pull E/D type driver, and

(b) address decoder with dynamic E/D circuit and push-pull E/D type driver.

In Fig. 4.26 (a), both gate-drain connected load and gate-source connected load are shown for address decoder. The former circuit is designed in the same manner as the enhancement-load circuit. The design for the latter circuit has been discussed in the previous sections. Hayashi et al. have also reported the design. [18]

The address driver is a positive buffer. When the gate voltage of the transistor Q_{DRD} is high, the gate voltage of Q_{DRL} is low, and vice versa. Therefore, this circuit is designed to have a β_R of around unity. The advantage of the circuit over conventional bootstrap circuit exists in the fact that during the period of charging C_A, the gate voltage of Q_{DRL} is equal to the supply voltage. That is, the effective gate voltage of the load transistor is $V_{DD} + |V_{TL}|$. This is larger than the case of bootstrap circuit in that the effective gate voltage is $V_{DD} - 2V_{TD}$.

The design of the E/D type buffer has been reported by Hayashi et al. for negative type buffer. [19] Similar method can be applied to the case of positive buffer. Since this is dynamic memory application, care should be taken with the low-level voltage V_{WL} at the write address. This is a specific problem for the address driver utilizing depletion type load. Thus the value of β_R should be designed so that the low-level voltage V_{WL} satisfies the relationship (4.34).

In Fig. 4.26 (b), the dynamic E/D adress decoder is used. This circuit works as follows. First, the transistor Q_{AL} charges the capacitor C_{AD}. Then, if the address is selected, the charge accross the capacitor C_{AD} is not discharged. If the address is not selected, the charge is discharged through the transistor Q_{DRD}. This circuit differs from the enhancement-load dynamic circuit in that;(1) the drain of the load device must be connected to the dc-supply, whereas it can be connected to the pulse supply in the case of enhancement-load dynamic circuit, and that (2) the low level voltage appears at the output node because the depletion load is conductive when the gate pulse is low. This low-level voltage is approximately given by

$$V_{ON} \simeq V_{TL}^2 / [2\beta_R (V_{DD} - V_{TD})], \qquad (4.35)$$

Figure 4.27 illustrates the output waveforms obtained from computer analysis for these circuits. The results indicate that the delay is almost half as small in the dynamic E/D type address decoder. The voltage loss seen in the figure arises from too short precharge time, and can be eliminated by employing a longer precharge time.

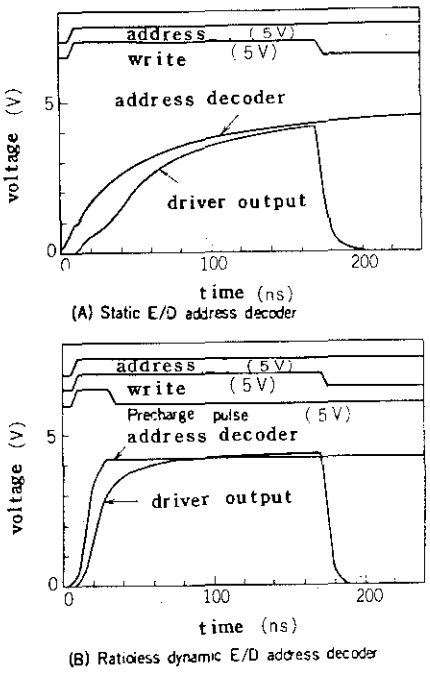


Figure 4.27 Computer calculated responses for the proposed addressing circuits.

4.3.4 Computer Analysis of the Entire Memory Circuit

To make possible computer analysis of the entire memory circuit, we consider a very simplified signal path. This is illustrated in Fig. 4.28.

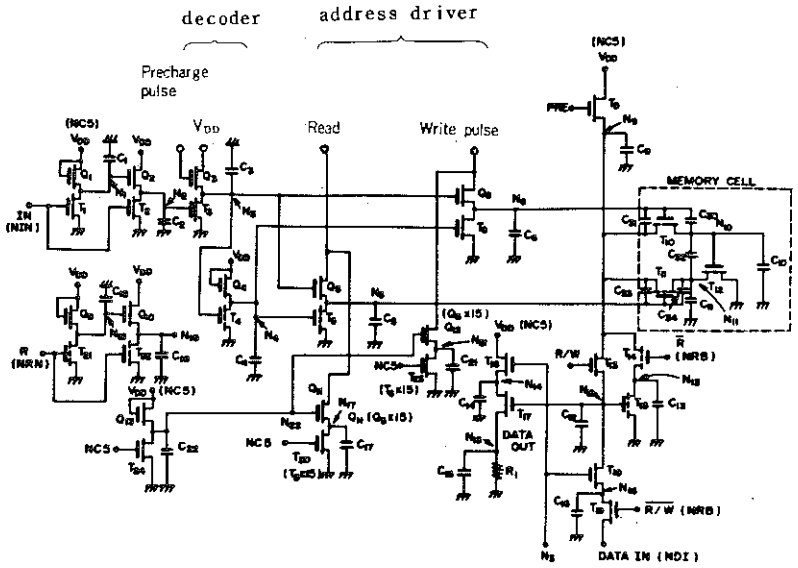


Figure 4.28 A schematic circuit for the computer calculation of the entire memory.

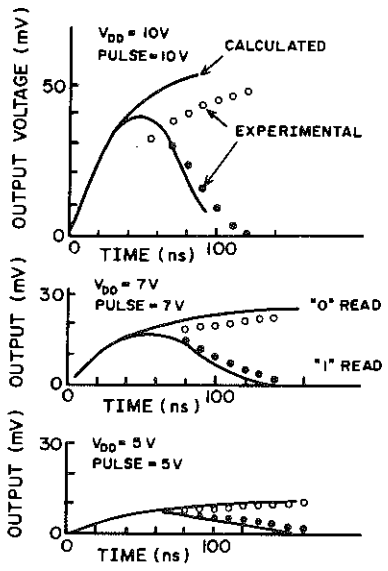


Figure 4.29 Comparison of the output waveforms of the computer calculation with experiments.

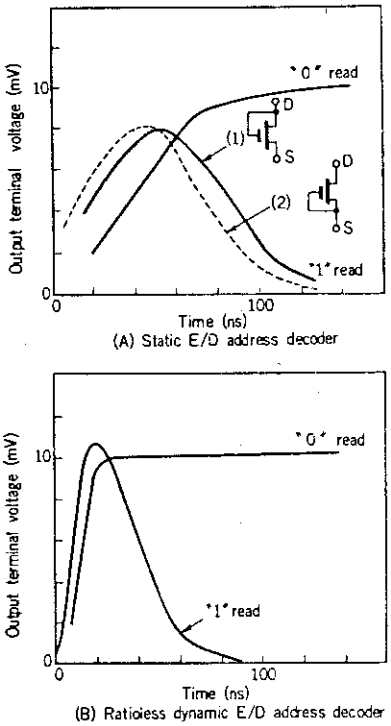


Figure 4.30 Comparison of the output waveforms by computer analysis.

(A) Static E/D address decoder.
(B) Dynamic E/D address decoder.

The circuit includes the addressing circuit, one memory cell and the sense amplifier. The size of the circuit is 37 FETs, 27 capacitors and 2 resistors. Figure 4.29 shows the comparison of the output waveforms between the calculation and the measurements. The measurements were done by using a 256-bit array using gate-drain connected static address decoder. The array was fabricated by the same process described in Section 4.2. In Fig. 4.29, the vertical axis indicates the output voltage of the 50-ohm load resistor. "1" corresponds to the low level at the output node because the data are inverted by the sense amplifier. The comparison shows that the agreement is good when the supply voltage is low.

Figure 4.30 shows the calculated output waveforms for the circuits using; (1) the static E/D decoder, (2) the dynamic E/D decoder. It is seen that the access time obtained in the case (b) is about half of that obtained in the case (a). This correlates with the previous result obtained for the charging time in each circuit as shown in Fig. 4.29. This fact suggests that the delay due to address decoder is dominant in the access time of the entire array. This is a specific feature of the present construction of the array, that is, the delay due to the address driver is minimized by employing the push-pull E/D type driver.

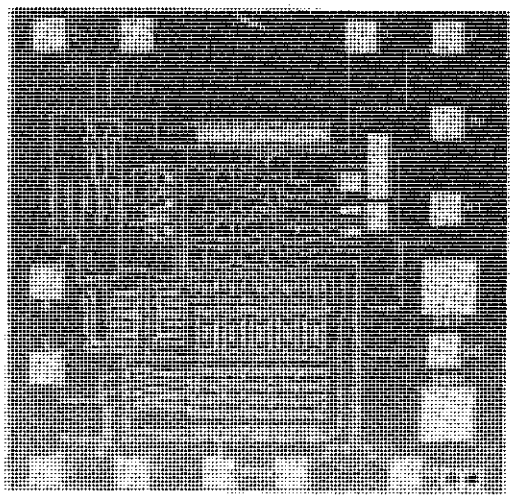


Figure 4.31 Microphotograph of the fabricated array.

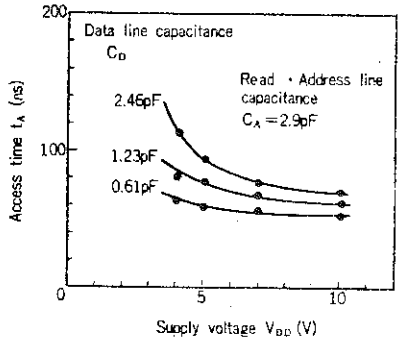


Figure 4.32 Access time t_A versus supply voltage V_{DD} for the fabricated test circuit with dynamic E/D address decoder and push-pull E/D address driver.

4.3.5 Experimental Results

Experimantal random-access memory has been fabricated based on the design considerations described in Section 4.3.4. The memory array was fabricated by the n-channel technology described in Section 4.2. Figure 4.31 shows the microphotograph of the chip to measure the access time for various cell designs. Thus the chip consists of memory cells with different designs, input buffer, address decoder, read and write address drivers and sense and refresh amplifiers. Dummy capacitors are added to the address and the data lines to simulate the access time in large arrays. 256-bit array was also made on the same mask pattern.

Figure 4.32 illustrates the total access time obtained for the chip as a function of the supply voltage. It is seen that the array operates with a supply voltage as low as four volts without a significant increase of access time. The increase of access time observed is attributed to the decrease of the high level voltage in memory cells. The estimated power consumption of the array was 0.04 mW/bit assuming a one kilobit array in read and write mode. This is considerably smaller value than that obtained in arrays with high supply voltages. Further decrease of the power is possible by the dynamic operation of other peripheral circuits and the use of improved photolithography.

From the preceding results it is concluded that the push-pull E/D type address drivers and the dynamic E/D address decoder are effective for +5-volt single supply random-access memories.

4.4 Conclusion

Design of static and dynamic E/D (depletion-load) circuit has been discussed. A design approach to optimize the dc-transfer curves in E/D static inverter was proposed from the viewpoint of obtaining a high noise immunity. Power and delay time of the E/D inverter have also been discussed. It was shown that the circuit operates with supply voltages as low as 1.5 volts, and the delay-power product is 15 ns/pF at 5 volts and 1.5 pJ/pF at 1.5 volts.

Design of a dynamic random-access memory having E/D type address circuits was presented. The circuit performances of several types of E/D addressing circuits were compared. It was pointed out that the use of push-pull address drivers and a dynamic E/D address decoder will give the best access time. A threshold voltage design for MOSFETs in a low-voltage memory array was discussed for the purpose of having enough refresh time.

Experimental arrays were fabricated to compare the design theories with experiments and to demonstrate the feasibility of these E/D configurations. The fabricated circuits were;(1) single NOR gate , (2) 2048-bit read-only memory utilizing static E/D inverters and (3) prototype random-access memory utilizing dynamic E/D circuits. These arrays were successfully operated with five-volt single supplies, and the inputs and outputs were TTL compatible except the output and pulse inputs of the random-access memory.

The design approaches discussed so far are general, and can be applied to any device fabrication technologies. For instance, threshold voltage control by ion-implantation and substrate bias, p and n-channel, metal gate and silicon gate are covered because the threshold voltages, conductances and subthreshold characteristics are the essential design parameters in the present design theories.

CHAPTER 5 A NEW CMOS DEVICE AND PROCESS

5.1 Introduction

The advent of very large scale integrated circuit such as 100 kilobit memories or 10 kilogate logic circuits has brought heightened focus to circuit designs having very low standby power dissipation. Complementary MOS (CMOS) circuits with their extremely low standby power are, therefore, very attractive. A second advantageous aspect of CMOS circuits is that they offer compatible fabrication together with high gain amplifiers, comparators and other analog functions on a single chip.

Balanced against these advantages, however, is a more complex process than that needed to produce MOS devices of only one type. Figure 5.1 illustrates a typical metal gate [1] and a silicon gate [2] CMOS process. It is seen that the metal gate process needs six masks, and the silicon gate process needs seven masks. Both processes need three diffusions, and the well diffusion takes 15 to 16 hours. These facts show that the CMOS processes are rather complex in compared to standard n-channel process that needs essentially four to five masks, and does not require such long diffusion step. The added complexity results in low circuit density and relatively smaller yield for CMOS integrated circuit.

The intent of this chapter is to propose a new CMOS technology that features in very simple processing and high packing density. The basic n-channel device used here is a symmetrical DMOS transistor, in that the channel doping is increasing toward both the drain and the source. Thus, the DMOST differs from the conventional DMOST having asymmetrical dopings.

The processing and the experimental results of the CMOS device will be presented in Section 5.2. Then, analysis and design of the DMOST will be discussed in Section 5.3.

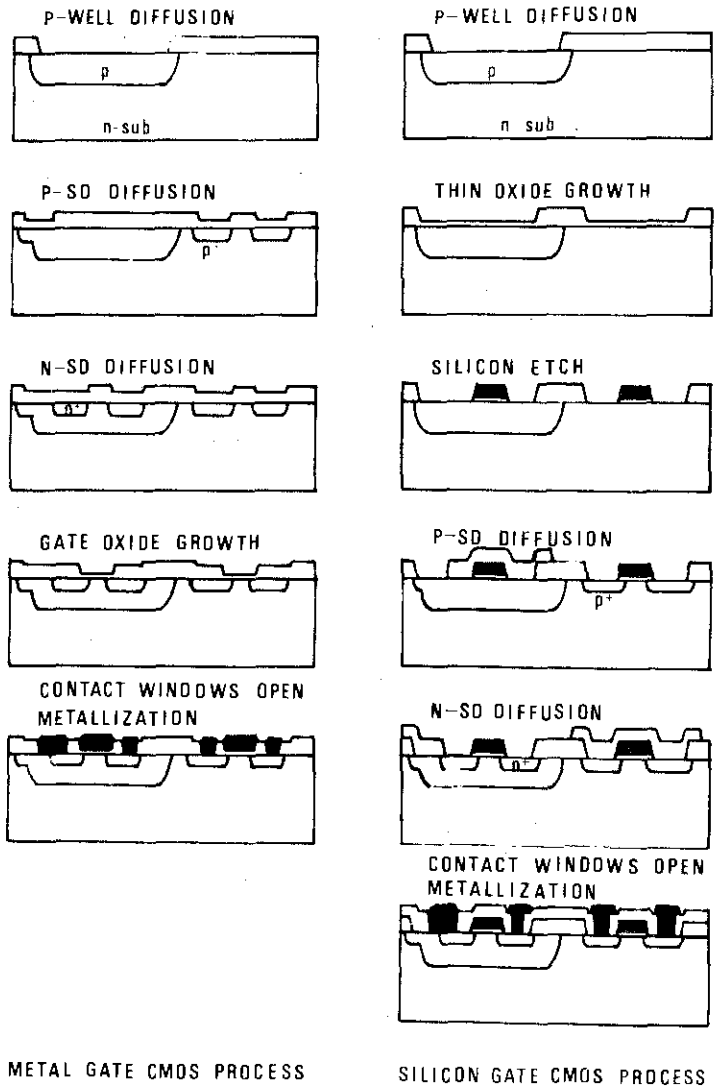


Figure 5.1 Typical metal gate and silicon gate CMOS processing steps.

5.2 CMOS Process Using Symmetrical Double-Diffused MOSFET

5.2.1 Double-Diffused CMOS Integrated Circuit

Figure 5.2 represents schematically the fabrication steps for the double-diffused CMOS integrated circuit process. The starting material is n-type (100) silicon with a resistivity of 1 to 3 ohm.cm. The procedures in each step are as follows.
(1) After the wafer is oxidized, source and drain windows for the n-channel devices are opened. Boron is deposited through these either by ion-implantation or by high temperature pre-deposition. The boron diffusion is continued until both the source and the drain regions merge to form a single p-well region.
(2) Arsenic is implanted through the same windows as were used for the process step (1), and then diffused. This step makes n^+ layers for the source and the drain of n-channel transistors. Arsenic is chosen because it has a much smaller diffusion constant than boron. The n^+ layers will not, therefore, penetrate through the p-regions during subsequent high temperature treatments.
(3) Source and drain windows for p-channel devices are opened. P^+ contacts for biasing the p-well is made at the same time. Boron is diffused

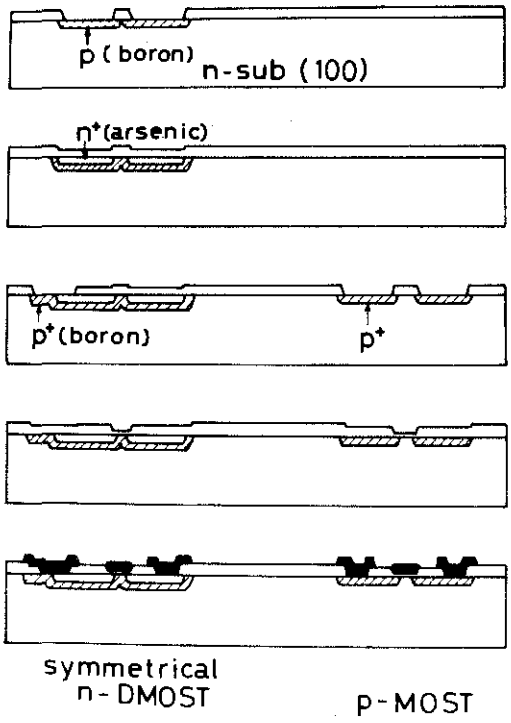


Figure 5.2 Processing steps for the double-diffused CMOS.

through these windows.
(4) Gate windows are opened and a thin gate oxide is grown.
(5) Contact windows for transistors and p-well are opened, and the device is finally metallized.

The advantages of the proposed CMOS technology are:
(1) Only five masks are required, fewer than for any existing CMOS technologies. [1], [2]
(2) No alignment is necessary between the p-well diffusion and the source and the drain diffusions of n-channel devices.
(3) The p-well diffusion can be thinner than that used for standard CMOS. This reduces the diffusion time, and also the processing cost of the wafer.
(4) Short channel devices which do not have punch-through problems are possible for n-channel transistors. This is the case because the total acceptor dopant between the source and the drain is higher than would be the case in standard CMOS. Furthermore the source junction is shielded by a double diffused p-layer. The punch-through voltage is therefore correspondingly increased.
(5) Higher packing density than that for conventional CMOS owing to the advantages enumerated under numbers (2), (3) and (4). Layout of the CMOS structures is also facilitated because it is not necessary to group n-channel devices into a large single p-well.

Figure 5.3 shows a schematic comparison of the size of the n-channel devices fabricated by standard CMOS technology and the double-diffused CMOS technology. The vertical scale is doubled as compared to the horizontal scale. It is clear that the p-well size is much smaller in the double-diffused device.
A brief comparison of the two technologies is summarized in Table 5.1.

Table 5.1.

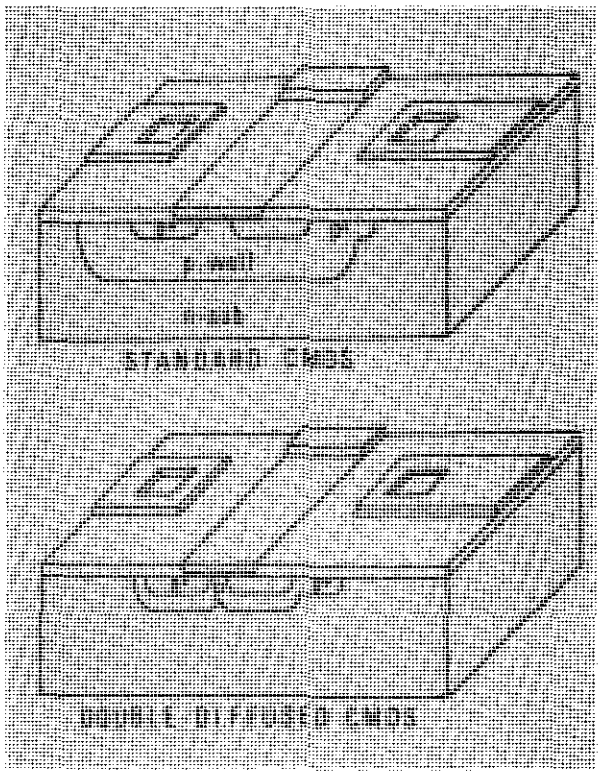


Figure 5.3 Comparison of the size of n-channel devices. Vertical scale is doubled as compared to the horizontal scale.

Table 5.1 Comparison of CMOS technologies.

	STANDARD	DOUBLE DIFFUSED
NUMBER OF THE MASKS	6 – 7	5
WELL DIFFUSION	16 hrs	3 hrs.
WELL AREA	100	50
INVERTER CELL AREA	100	70
GROUPING OF N MOST	NECESSARY	NOT NECESSARY

5.2.2 Device Fabrication

A prototype integrated circuit has been fabricated to demonstrate the feasibility of the technology. Figure 5.4 illustrates a microphotograph of the fabricated chip. This includes p, n-channel transistors, bipolar transistors with substrate as a collector and a seven stage inverter chain. Typical layout rules are; six microns for source to drain spacings, 12 microns for the spacings between p and n-channel transistor source and drain diffusions. These design tolerances are just for the convenience in fabrication and do not correspond to

the device limitation. It appears that shorter channel lengths and the corresponding reduction of well depth makes possible much tighter tolerance.

Two series of runs have been carried out. The first run-series employed a high temperature predeposition of boron from a diborane source for both the p-well and for the source and drain diffusion of the p-channel devices. This process produced some operating circuits, but threshold control for the n-channel transistors was not good. The second run series used ion-implantation of boron for these two steps, as well as for the n^+ source and drain depositions. The processing steps for the second run series are illustrated in Table 5.2.

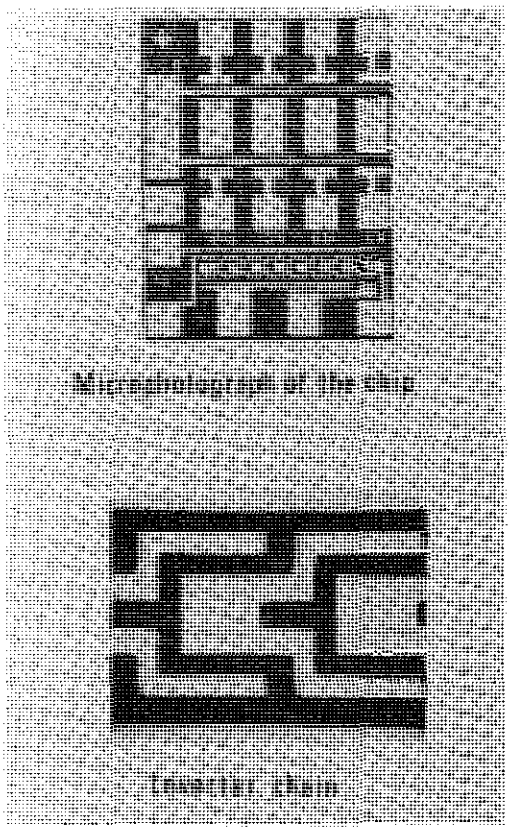


Figure 5.4 Microphotograph of the fabricated chip.

Table 5.2 Processing steps in the second run series that employed ion-implantation for all the deposition steps.

PROCESSING STEPS	
1. INITIAL OXIDE GROWTH	
2. N-SD WINDOWS OPEN	(MASK NO.1)
3. BORON IMPLANT	
4. BORON DIFFUSION	1200 °C, 2 hrs. in N_2
5. ARSENIC IMPLANTATION	100 KeV, 4×10^{15} cm^{-2}
6. ANNEAL AND ARSENIC DIFFUSION	1200 °C, 1 hr. in N_2
7. P-SD WINDOWS OPEN	(MASK NO.2)
8. BORON DEPOSIT AND DIFFUSION	
9. GATE WINDOWS OPEN	(MASK NO.3)
10. GATE OXIDE GROWTH	1050 °C, 40 min. in dry O_2
11. CONTACT WINDOWS OPEN	(MASK NO.4)
12. AL METALLIZATION	(MASK NO.5)

In the step (3) of this run series, implantation conditions were varied from 1×10^{13} cm^{-2} to 3×10^{14} cm^{-2} at 30 KeV in order to find a proper dose for the p-well. For the first run series, boron predeposition in step (3) had been done in a boron predeposition furnace at 875°C for 30 min., and step(8) also used the same method. The results from the second run series were superior and the discussion of measurements will emphasize them.

Figure 5.5 shows a stained surface after the formation of the p-well and the n^+ source and drain diffusions. The top right figure corresponds to the p-well and n^+ diffusions that exist in the inverter chain. The top-left figure is a closer view of the top-right figure. The white regions are n^+ source and drain diffusions, and the dark region surrounding the n^+ regions is the p-well. An angle-lapped and stained cross section is also shown in the figure. Side diffusion parameters have been measured from the stained patterns and the results are given in Table. 5.3.

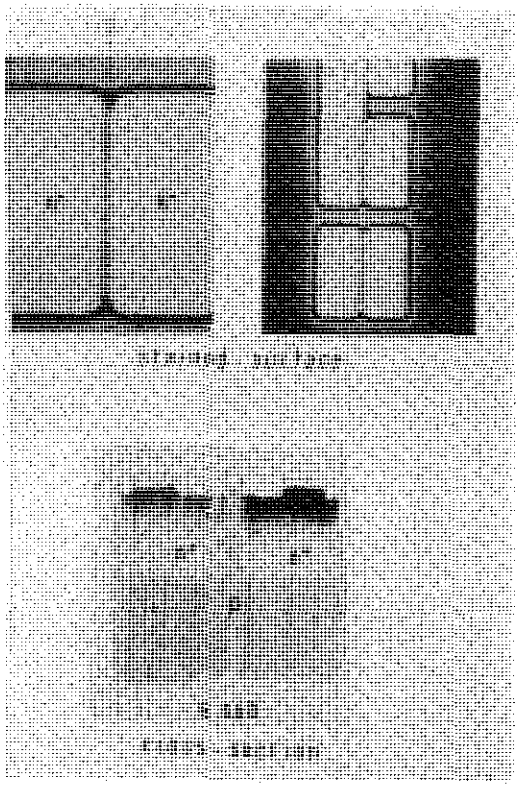


Figure 5.5 A stained surface and cross-section after the formation of p-well and n^+ diffusions. The white regions in the surface pattern are n^+ arsenic diffused layers, and dark regions are p-wells.

Table 5.3 Measured diffusion parameters.

Mask SD spacing	6.7 μm
Boron side diffusion	3.6 μm
Arsenic side diffusion	1.8 μm
Actual SD spacing	3.1 μm

Special care was taken in determining the diffusion characteristics because; (1) to produce the double-diffused CMOS circuits, the side diffusion of boron should be at least half of the source to drain spacing of n-channel devices on the mask, and (2) the threshold voltage is determined by the boron concentration at the source edge of the p-well. Thus, not only the total boron dose, but also the diffusion conditions for both boron and arsenic enter into the determination of the threshold voltage. The diffusion conditions for the present study shown in Table 5.3 were determined for a mask source to drain spacing of six microns. For closer spacing, diffusion time and/or temperatures would need to be modified in order to obtain the same threshold voltage.

5.2.3 Measured Transistor Characteristics

Drain current vs. drain voltage curves for n and p-channel MOS transistors, and collector current vs. collector voltage curves for the associated bipolar transistor with n-substrate as a collector, are shown in Fig. 5.6. The bipolar transistor is useful when one wants to drive a large capacitance. These curves are for the second-run-series wafer with a boron dose of $1 \times 10^{14} cm^{-2}$ for the p-well predeposition.

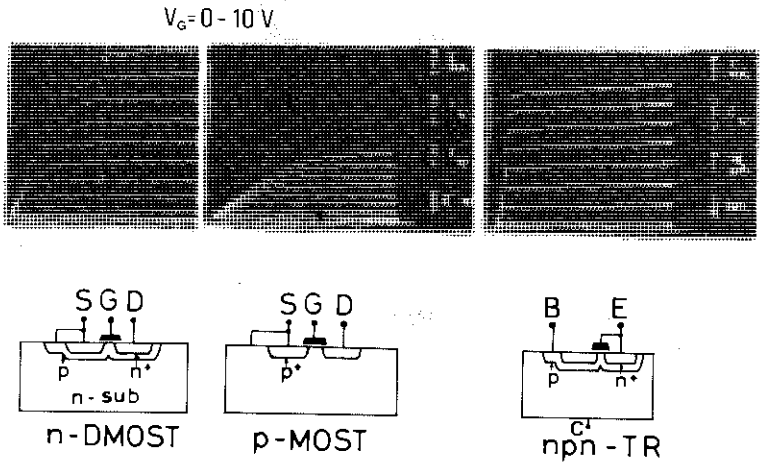


Figure 5.6 Drain current versus drain voltage curves and collector current versus collector voltage curves for the samples with 1×10^{14} cm^{-2} boron dose for the p-well predeposition.

By varying the dose, the threshold voltage and the transconductance of n-channel transistors, the current gain of bipolar transistors and the breakdown voltage between p-well and the drain of n-channel devices vary significantly. Drain current vs. drain voltage curves for n-channel transistors with different p-well predeposition dose are shown in Fig. 5.7. The apparent leakage current in the device with a dose of 3×10^{13} cm^{-2} occurs because the transistor is in the depletion mode which permits a leakage current between n-substrate and n^+ diffusion.

It should be noted that in spite of the fact that the n-channel device has a source to drain spacing of around three microns, the transistor does not exhibit typical short-channel effects such as threshold variation due to the drain voltage variation, low drain resistance in the saturation region, and the occurence of the punch-through effect. It has been shown previously that a channel length of one micron can be achieved without threshold lowering effect by using asymmetrical double-diffused MOSFET [58]. The preceding result indicates that the proposed symmetrical double-diffused transistor also makes possible a short channel device. Further experiments are now under way.

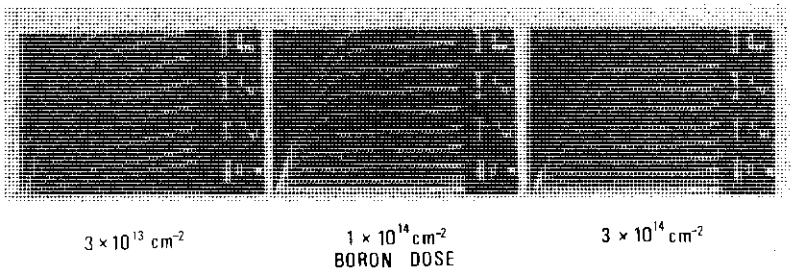


Figure 5.7 Drain current versus drain voltage curves for the n-channel transistors with differing boron dose for the p-well.

Figure 5.8 shows the threshold voltage variations in these samples measured accross the wafers. The average threshold for the p-channel device is -1.8 volts. For the n-channel devices, the average threshold is 0.2 volts for a p-well boron dose of 1×10^{14} cm^{-2}, and 1.2 volts for 3×10^{14} cm^{-2}. The variation is seen to be larger in n-channel devices.

The breakdown voltage is 17 volts for devices made with a 1×10^{14} cm^{-2} p-well dose and is 12 volts for these having a 3×10^{14} cm^{-2}. The value of bipolar current gain β is 20 to 100 for 1×10^{14} cm^{-2}, and 20 to 25 for 3×10^{14} cm^{-2}.

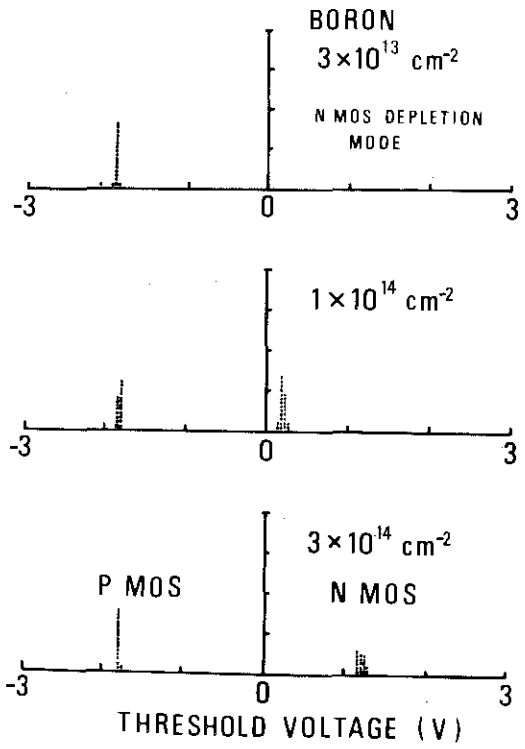


Figure 5.8 Threshold voltage variations for various p-well doses.

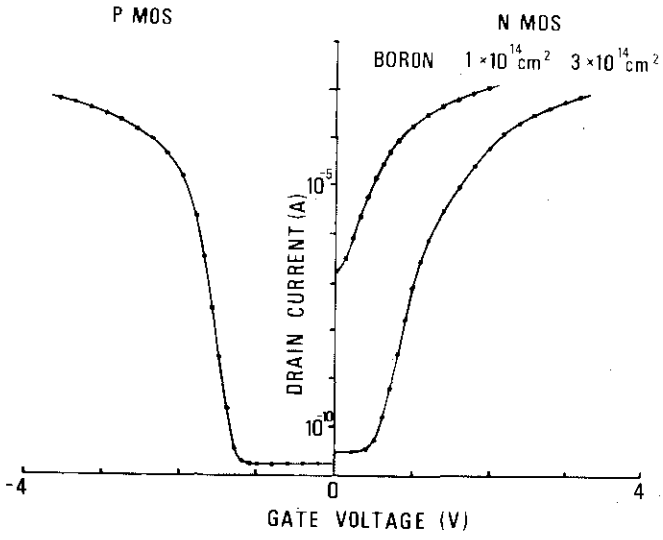


Figure 5.9 Subthreshold characteristics of MOSFETs.

Figure 5.9 shows subthreshold characteristics of the transistors. This figure reveals that in order to operate the CMOS circuits in a dynamic mode, a dose of 1×10^{14} cm^{-2} is insufficient because considerable amount of subthreshold tail current exists when the gate voltage is zero. In the n-channel transistors with 3×10^{14} cm^{-2} p-well dose, the shape of the log I_D - V_G curve at the current level of 10^{-7}A to 10^{-4} A is somewhat different from that of standard MOS transistor that was measured in Section 3.2. This arises from the non-uniform boron doping along the channel. That is, the transistor has higher threshold voltage at the source and the drain end of the channel, thus, effective channel length becomes shorter with decreasing the gate voltage because the effect of the difference of threshold voltage on channel conductance at each position in the channel becomes larger at low gate voltages. One of the problems in the present devices is that the value of the current at zero gate voltage is large by one to two orders in compared to the standard device. Further modification of the processing appears necessary on this point.

The symmetrical n-channel double-diffused MOSFET discussed so far has a p^+ diffusion for biasing the p-well to the same potential as source. Figure 5.10 shows the difference of I_D - V_D curves for the device

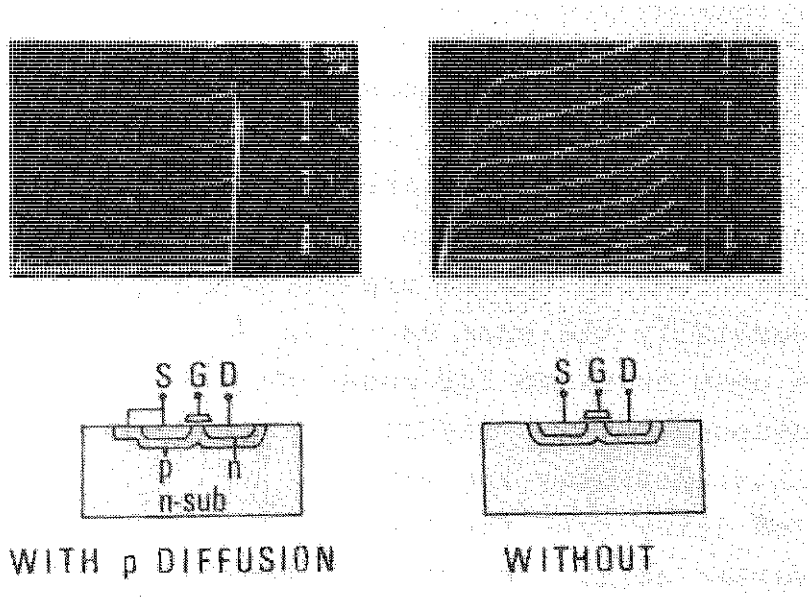


Figure 5.10 Drain current versus drain voltage curves for devices with and without the p^+ diffusion for biasing the p-well.

with and without the p^+ diffusion. It is seen that current kinks are observed in the device that does not have the p^+ diffusion. This is associated with the fact that the p-well is floating. That is, once weak avalanche occurs at the drain depletion layer, the hole current charges up the p-well to a slightly positive voltage. Then it happens that the drain voltage is above a certain value, a lateral bipolar transistor is activated, and excess current is added to the normal drain current. This mechanism is exactly the same as the kinks observed in a silicon-on-sapphire MOS transistor in that p-substrate is also floating. [5], [6] Since the current kinks occur at three to five volts depending on the gate bias, it is possible to eliminate the p^+ diffusion for devices operated with supplies below two volts. This will further reduce the area for n-channel transistors.

5.2.4 Circuit Performance

Measured inverter transfer curves are shown in Fig. 5.11. The inverter consists of n and p-channel transistors with channel widths of 125 μm and mask source to drain spacings of six microns. These transfer curves are essentially the same as the ones obtained for conventional CMOS. Figure 5.12 illustrates the measured delay time for the inverter cell. The measurements were carried out by using a seven stage

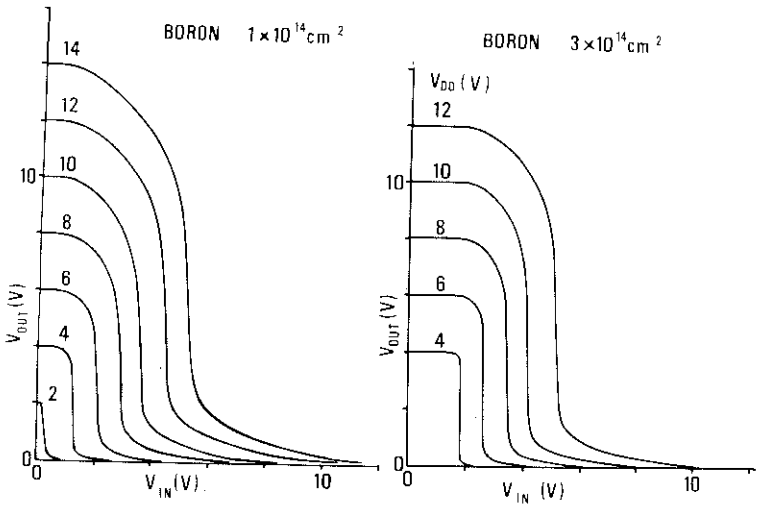


Figure 5.11 Dc-transfer curves for the double-diffused CMOS inverter.

chain of inverters followed by a source follower circuit with 50 ohm load resistor. The channel widths for the cell of the chain were 62.5 μm for both devices and source to drain spacings were also six microns. In ion-implanted wafers, typical delay/stage is 8 to 13 nanoseconds at 5 volts and it is 4 to 5 nanoseconds at 10 volts. The relativaly large delay in the high temperature predeposited wafers in the first run series arises because the boron concentration at the n^+-p junctions is high. This results in increased junction capacitance and higher threshold voltage. The threshold for the first run series was approximately two volts and the drain breakdown voltage was 9.5 volts. In the second run series, special care was also taken with wafer cleaning and annealing after ion-implantation. This resulted in a lower surface-state density and a higher mobility.

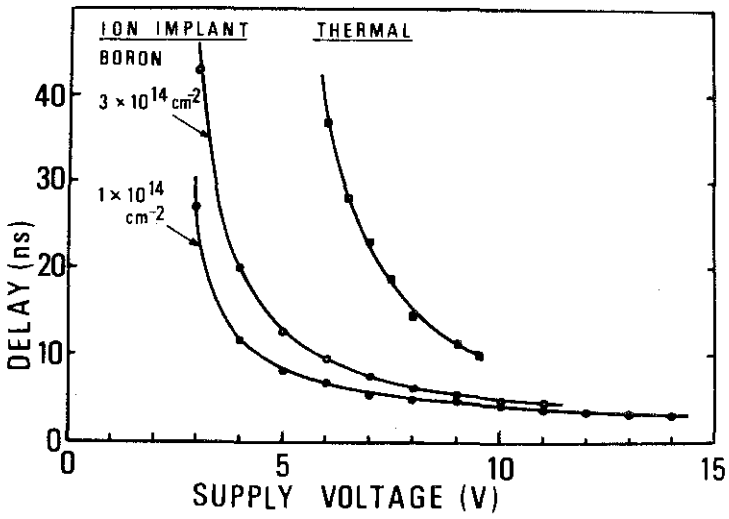


Figure 5.12 Delay time/stage of the inverter as a function of the supply voltage. The curve marked "Thermal" was measured on devices made with high temperature predeposited boron p-wells in the first run series.

5.3 Analysis and Design of Symmetrical Double-Diffused MOSFET

The numerical analysis of the double-diffused MOSFETs discussed in Section 3.5 was applied to the analysis of the symmetrical double-diffused MOSFET used in the proposed CMOS. Figure 5.13 is a comparison of the results of the analysis with the measurements for the device with a boron dose of 3×10^{14} cm^{-2} for the p-well. The agreement is seen to be good when the gate voltage is low and when the device is in non-saturation region. However, at high gate voltage and in saturation region, the analysis predicts lower current than the measurement. This is attributed to an incorrect assumption of the velocity-field relationship in the analysis, because the saturation of the current in short channel devices is determined by the velocity saturation.

Figure 5.14 shows variations of quasi-Fermi potential and mobility along the channel in the device shown in Fig. 5.13. Generally, the shape of the potential curves is similar to that of conventional MOS transistor in that the field is highst at the drain end of the channel. However, high field region is again seen at the source end. Corresponding to the high field and high concentration region, the mobility is low at the source end and the drain end of the channel.

To perform a better comparison, drain current versus drain voltage curves and variations of potential and mobility were calculated for a conventional MOSFET having a substrate doping concentration that is equal to the doping at the source end in the symmetrical DMOSFET. These results are shown in Figs. 5.15 and 5.16. The comparison of the potential distribution in the two devices indicates that a high field region at the source exists only in the double-diffused MOSFET. This feature was also seen in the

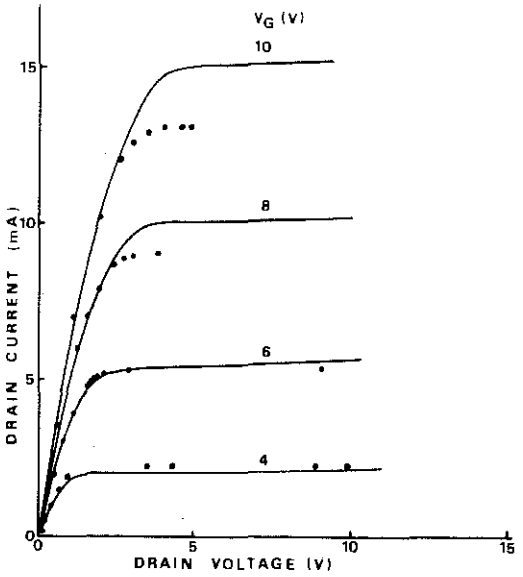


Figure 5.13
Comparison between the theory and measurements of drain current versus drain voltage curves for p-p⁻-p type symmetrical DMOSFET. Dots represent theory.

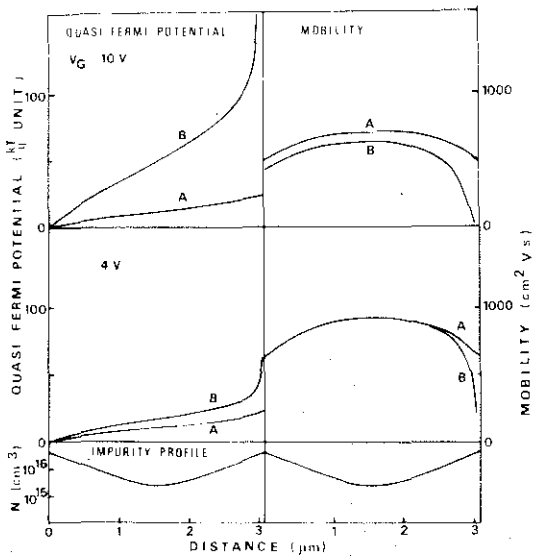


Figure 5.14 Quasi-Fermi potential and mobility variation for the device shown in Fig. 5.13. $\mu_{max}=1200 cm^2/V.s$ and $\theta = 0.12\times10^{-8} m/V$ are assumed.

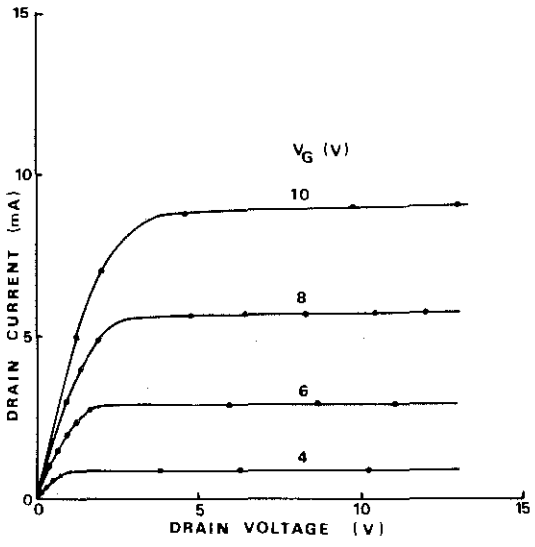


Figure 5.15 Calculated drain current versus drain voltage curves for the conventinal MOSFET having a substrate doping equal to the p-region doping at the source end in DMOSFET shown in Fig. 5.13.

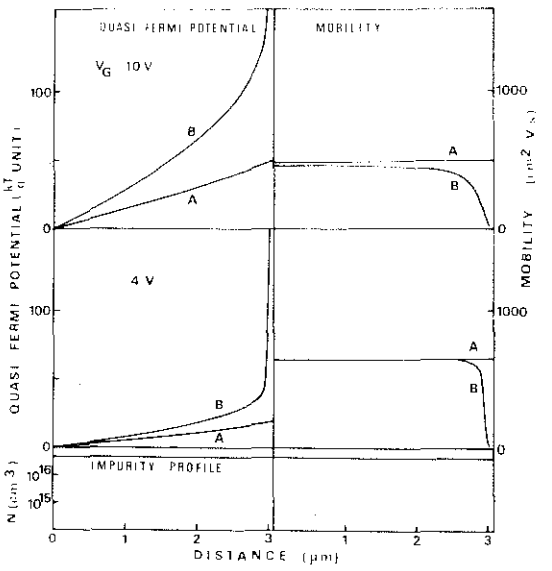


Figure 5.16 Quasi-Fermi potential and mobility variations along the channel for the device shown in Fig. 5.15.

asymmetrical DMOSFET. In both cases a highly doped region in the vicinity of the source junction causes the high field region because the threshold voltage is highest there.

The high field obtained in the double-diffused MOSFETs results in a higher current than that for standard type MOSFET. This is because the current is determined by

$$I_D = \mu q N E_y \ (y=0) \ . \qquad (5.1)$$

The calculated curves in Figs. 5.13 and 5.15 show that the value of the current in the symmetrical double-diffused MOSFET is approximately twice as high as that of the standard MOSFET when the gate voltage is low, for instance, at four volts.

The behavior of the symmetrical double-diffused MOSFET, however, differs from the asymmetrical ones when the device is biased near or above pinch-off condition. For example, the pinch-off voltage for the device shown in Fig. 5.13 is approximately 2.2 volts when the device is biased at $V_G = 6$ V, whereas the asymmetrical MOSFET shown in Fig. 3.42 exhibits a pinch-off drain voltage of around 4.5 volts in the same bias condition. The reason for this is that the pinch-off of the channel depends mostly on the doping density near the drain junction. Thus, the pinch-off voltages shown in Fig. 5.13 are almost identical to those for MOSFET with uniformly doped substrate as shown in Fig. 5.16. Consequently, the saturation current is higher for asymmetrical double-diffused MOSFET than for symmetrical double-diffused MOSFET.

The preceding discussion indicates that if one designs a symmetrical MOSFET for use in the present CMOS circuit so that the channel conductance would be as high as possible, it is desirable to have a doping profile that has a low doped region in the middle portion of the channel, because a high mobility and a low threshold voltage, in other words, a high channel conductance is expected in that portion.

In actual cases, the doping of the symmetrical device for use in the present CMOS should be determined assuming a parasitic MOS transistor that exists between the n^+ diffusion and the substrate. Figure 5.17 shows some of the design considerations for the parasitic MOS transistor. The left figure indicates a cross-section of the symmetrical double-diffused MOSFET toward the direction along the channel. The right figure indicates a cross-section at the middle portion of the channel toward the direction perpendicular to the cross-section 1. In the cross-section 1, it is required that the depletion layer underneath the channel should not exceed tha depth of the p-well region. Once this happens, a large leakage current flows from the substrate, that usually is biased to the highest potential, to the source n^+ diffusion. A critical point is the central portion of the channel where two well diffusions from the source window and the drain window merge. Thus, the condition $x_{min} > x_{dep}$, must be satisfied at any bias conditions.

It should also be noted that another parasitic effect occurs in cross-section 2. This is a double-diffused MOS transistor with the substrate as a drain and with the channel as a source. The threshold voltage of the parasitic MOS transistor is determined by the doping N_{min} at the center of the channel and the thickness T_{OXF} of the field oxide. This is because the transistor has the inversion layer as a source, and the threshold voltage in such DMOSFET is determined by the doping at the edge of the source diffusion.

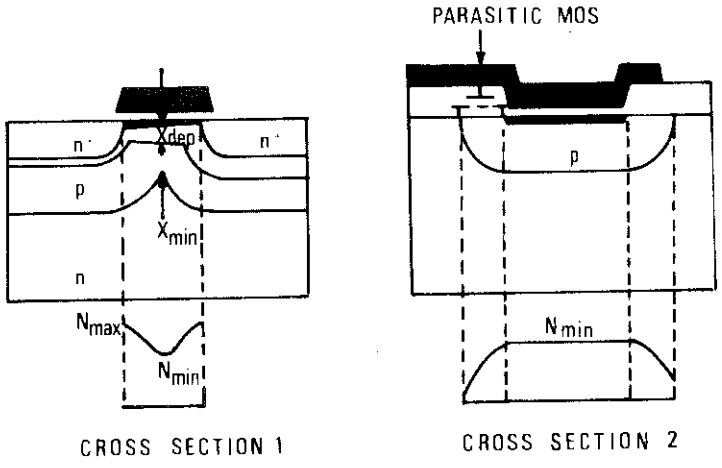


Figure 5.17 Cross-sections for the double-diffused MOSFET. The left figure shows a cross-section along the channel. The right figure shows a perpendicular cross-section in the middle portion of the channel.

Therefore, the doping N_{min} should be determined so that the threshold of the parasitic MOSFET would be higher than the gate voltage, especially when the circuit needs to be operated with a low power dissipation. In some cases the existance of the parasitic MOSFET is allowed because the parasitic MOSFET has considerably low transconductance and does not affect the circuit operation. However, in such cases, one has to allow additional power dissipation due to the parasitic MOS when the inverter output is low.

5.4 Conclusion

A new CMOS integrated circuit technology that utilizes a symmetrical double-diffused n-channel MOSFET has been demonstrated. Features of the technology are the use of five masks, a self aligned p-well diffusion and short channel n-channel transistors. These result in a fifty percent reduction in the p-well area as compared to conventional CMOS devices and lowers the processing costs.

Integrated circuits, fabricated using boron implantation for the p-well dose and p^+ diffusion, and arsenic implantation for the n^+ diffusion, exhibit a p-channel threshold of -1.8 volts and an n-channel threshold of 1.2 volts with a p-well dose of 3×10^{14} cm^{-2}. An inverter chain of seven cells has been operated with a supply of 3 to 11 volts. In operation, the delay per stage was measured to be 13 ns at 5 volts and 5 ns at 10 volts.

The analysis and some design consideration of the symmetrical n-channel double-diffused MOSFET was presented. It was shown that the proposed device has higher transconductance than standard MOSFET at low gate bias.

CHAPTER 6 CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY

MOSFET models and analyses for low voltage MOS integrated circuits, properties of enhancement-deplation (E/D) static and dynamic circuits, and a new simplified CMOS process have been studied throughout the thesis.

It was revealed that increased power delivered to large-scale integrated circuits sets a practical limit to the density of the integration. Maximum gate number in logic circuits or bit numbers in memory circuits are determined by the power dissipation.

A general approach to reduce the power dissipation is to decrease the supply voltage. This makes it necessary to investigate behavior of MOSFET near the threshold condition. An accurate and, at the same time, practical model that applies over a wide range of current including the subthreshold region must be developed. A new model for the standard MOSFET having a constant doping underneath the gate, was proposed for this purpose. This model utilizes analytical current equations divided into three operating regions for the MOSFET: the non-saturation region, the saturation region and the subthreshold or "tail-current" region. The equations are derived based on an accurate calculation of the surface potentials at the source end of the channel and at the pinch-off point. The comparison of the current-voltage characteristics between theory and experiments was performed for a wide range of oxide thicknesses (220 to 5030 Å), substrate doping densities (7×10^{13} to $4 \times 10^{15} cm^{-3}$) and temperatures (220 to 343 K). Good agreement was observed both in log I_D - V_G curves and log I_D - V_D curves in a current range 10^{-2} to 10^{-11}A.

In order ro reduce the voltage needed to operate MOS digital circuits, low threshold enhancement and depletion mode devices are desirable. Threshold control by ion-implantation was discussed from this point of view. It was shown that a single layer implantation makes possible threshold shifts in either the positive or

negative direction. However, the characteristics of the transistors at low currents are strongly influenced by the implantation condition. For instance, boron implantation in an n-channel device causes less steep log I_D-V_G curves in compared to unimplanted case. This places a significant limit on the use of low supply voltage because it is required that the threshold voltage should be higher than a certain level so that the transistor is completely off when the gate voltage is low. On the other hand, phosphorus implantation causes residual current. It was found that a double-layer implantation of impurities of differing species makes possible a nearly parallel shift of the log I_D - V_G curves. The double-layer implantation can also be used to realize MOSFETs having a residual current and less steep log I_D - V_G curves than standard devices. These features are realized independent of the control of the threshold voltage.

The double-diffused MOSFET (DMOSFET) has a number of advantages over conventional MOSFETs in low power applications. It realizes an effectively short channel without suffering from a number of effects associated with the shrinking of the channel length. These are; (1) threshold voltage variation with drain voltage and with variations of photolithography, (2) punch-through and low drain breakdown voltage. A numerical analysis of the DMOSFET dc-current vs. voltage characteristics was carried out. The analysis is based on: (1) accurate charge equations, (2) dependence of mobility on gate and drain field and doping. The analysis is capable of handling various DMOSFET structures. It was shown that the gradient of doping plays an important role for the field distribution of the device. This indicates that simple two-transistor model can not be applied. The comparison between the theory and experiments has been carried out using p-n type asymmetrical DMOSFET and $p\text{-}p^{-}\text{-}p$ type symmetrical DMOSFET. The agreement was quite good in the non-saturation region. In the saturation region descrepancies were observed. This was attributed to an inaccurate velocity-field relationship in the vicinity of the saturation velocity.

Design and experiments of enhancement/depletion (E/D) circuits were discussed. A general design approach for static inverters for the purpose of optimizing the dc-transfer curves was proposed. The emphasis of the design was on the operation at five volts and at 1.5 volts. The design indicated that the power-delay product will be as low as one picojoule for a load capacitance of 1 pF at 1.5 volts. Dynamic operation of the E/D configuration was proposed for addressing circuit of dynamic memories. This makes possible a fast access time of less than a hundred nanoseconds even with a single five-volt supply. A prototype read-only memory utilizing the static E/D inverter and a random-access memory utilizing the dynamic E/D decoder and push-pull driver were designed and fabricated. Both Al_2O_3/SiO_2 double layer enhancement-type devices and PSG/SiO_2 double layer depletion-type devices were integrated on a same chip. Both circuits were successfully operated with a single five-volt supply.

These circuit techniques will be of special importance in the integrated circuit that contains transistors of single type. The use of ion-implantation technique greatly increases the design flexibility.

Complementary MOS (CMOS) technology is attractive because of its low quiescent power dissipation. However, its very complex processing has resulted in a low yield and low circuit density. A new simplified CMOS process for large scale integrated circuit was proposed. This utilizes a symmetrical double-diffused MOSFET for the n-channel devices. The features of the new technology were : (1) the use of only five masks which is simpler than any existing CMOS technologies, (2) the avoidance of the need to align the p-well to the source and the drain diffusions of n-channel devices. This has made possible a fifty percent reduction of the cell size as compared to conventional CMOS processes. A detailed analysis of the n-channel symmetrical DMOSFET in the CMOS cell was also discussed.

It appears that the technologies discussed in this thesis will be utilized in combination with advanced lithography and processing in the future LSI. MOSFETs having channel length of even less than a micron will be developed. Thus, modification of the present analyses will be needed. The emphasis should be on : (1) inclusion of short channel effects, (2) more accurate velocity-field relationships for both electrons and holes under the influence of the gate field, (3) properties of the parasitic bipolar transistor. It will also be desirable to consider MOSFET structures that are insensitive to the shrinking of the channel length.

Further reduction of the supply voltage will extend the limit of integration density. It is expected that the operation of MOSFETs in the weak inversion region will become more and more important. Dynamic operation of the depletion-load MOS and of CMOS will greatly help to reduce power. Study on new circuit techniques in these areas will be one of the key points for large scale integration in the future.

REFERENCES

REFERENCES FOR CHAPTER 1

(1) J. E. Lilienfeld, "Method and apparatus for controlling electronic currents," U.S. Patent 1745175, Jan.28, 1930.

(2) O. Heil, "Improvements in or relating to electrical amplifiers and other control arrangements," U.K. Patent 439457, Dec. 1935.

(3) D. Kahng and M. M. Attala, "Silicon-silicon dioxide field induced devices," Solid-State Device Research Conf., Pittsburgh, Pa., June 1960.

(4) D. Kahng, "Electrical field controlled semiconductor devices," U. S. Patent 3102230, Aug. 1963.

(5) M. M. Atalla, "Semiconductor triode," U.S. Patent 3056888, Oct. 1962.

(6) F. M. Wanlass, "Metal-oxide-semiconductor field-effect transistors and microcircuitry," WESCON 1963.

(7) R. H. Dennard, F. H. Gaensslen, L. Kuhn and H. N. Yu, "Design of micron switching devices," Intl. Electron Devices Meeting, p.168, 1972

(8) R. G. Daniels and R. R. Burgers, "The electronic wrist-watch: An application for Si gate CMOSICs," 1971 ISSCC Digest of Tech. Papers.

REFERENCES FOR CHAPTER 2

(1) C. N. Ahlquist, J. R. Breirogel, J. T. Koo, J. L. McCollum W. G. Oldham and A. L. Rennige," A 16K dynamic RAM," 1976 ISSCC Digest of Tech. Papers, Feb. 1976.

(2) K. Itoh, K. Shimohigashi, K. Chiba, K. Taniguchi and K. Kawamoto, "A high speed 16K bit NMOS RAM," 1976 ISSCC Digest of Tech Papers, Feb. 1976.

(3) K. Yoshida, I. Yamazaki, K. Doi, H. Nozawa, T. Shibata and M. Ueno, "A 16 bit LSI minicomputer," 1976 ISSCC Digest of Tech.Papers, Feb. 1976.
(4) C. T. Sah and H. C. Pao, "The effects of fixed bulk charge on the characteristics of metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol. ED-13, pp. 393 - 409, Apr. 1966.

REFERENCES FOR CHAPTER 3

(1) S. R. Hofstein and F. P. Heiman, "The silicon insulated-gate field-effect transistor," Proc. IEEE, p. 1190, 1963.
(2) H. Schichman and D. A. Hodges, "Modelling and simulation of insulated-gate field-effect transistor switching circuits," IEEE J. Solid-State Circuits, vol. SC-3, pp. 285-289, Sept. 1968.
(3) T. E. Idleman, F. S. Jenkins, W. J. McCalla and D. O. Pederson, "SLIC- A simulator for linear integrated circuits," IEEE J. Solid-State Circuits, vol. SC-6, pp. 14-19, Feb. 1971.
(4) H. K. J. Ihantola, "Design theory of a surface field-effect transistor," Stanford Electronics Lab. Tech. Report, No. 1661-1, 1961.
or
H. K. J. Ihantola and J. L. Moll, "Design theory of a surface field-effect transistor," Solid-State Electronics, vol. 7, p. 423, 1964.
(5) C. T. Sah, "Characteristics of metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol. ED-11, p. 324, 1964.
(6) D. F. Bentchkowsky and L. Vadasz, "Computer-aided design and characterization of digital MOS integrated circuits," IEEE J. Solid-State Circuits, vol. SC-4, pp. 57-64, 1969.

(7) V. G. K. Reddi and C. T. Sah, "Source to drain resistance beyond pinch-off in metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol. ED-12, pp. 139-141, 1965.
(8) J. E. Schroeder and R. S. Muller, "IGFET analysis through numerical solution of Poisson's equation," IEEE Trans. Electron Devices, vol. ED-15, pp. 954-961, 1968.
(9) D. P. Kennedy and P. C. Murley, "Steady-state mathematical theory for the insulated-gate field-effect transistor", IBM J. Res. Develop., pp. 2-12, Jan. 1973.
(10) G. D. Hachitel and M. H. Mack, "A graphical study of the current distribution in short channel IGFETs", 1973 ISSCC Digest of Tech. Papers, pp. 110-111.
(11) D. Vandorpe, J. Borel, G. Merckel and P. Saintot, "An accurate two dimensional numerical analysis of the MOS transistor", Solid-State Electronics, vol. 15, pp. 547-557, May 1972.
(12) M. S. Mock, "A two dimensional mathematical model of the insulated-gate field-effect transistor", Solid-State Electronics, vol. 16, pp. 601-609, 1973.
(13) D. F. Bentchkowsky and A. S. Grove, "Conductance of MOS transistor in saturation", IEEE Trans. Electron Devices, vol. ED-16, pp. 108-113, 1969.
(14) J. R. Schrieffer, "Effective carrier mobility in surface space charge layers", Phys. Rev., vol. 118, p. 967, 1960.
(15) R. F. Greene, D. R. Frankel and J. Zamel, "Surface transport in semiconductors", Phys. Rev., vol. 118, p. 967, 1960.
(16) C. T. Sah, T. H. Ning and L. L. Tschopp, "The scattering of electrons by surface oxide charges and by lattice vibrations at the silicon-silicon dioxide interface", Surface Sci., vol. 32, p. 279, 1968.
(17) R. F. Pierret and C. T. Sah, "An MOS-oriented investigation of effective mobility theory", Solid-State Electronics, vol. 11, pp. 279-290, 1968.

(18) O. Leistiko, A. S. Grove and C. T. Sah, "Electron and hole mobilities on inversion layers on thermally oxidized silicon surfaces," IEEE Trans. Electron Devices, vol. ED-12, pp. 248-254, 1965.
(19) J. T. Chen and R. S. Muller, "Carrier mobilities at weakly inverted silicon surfaces," J. Appl. Phys., vol. 45, p. 828, 1974.
(20) R. H. Crawford, "MOSFET in circuit design", New York: McGraw-Hill, 1967.
(21) D. Frowman-Bentchkowsky, "On the effect of mobility variation on MOS device characteristics," Proc. IEEE, vol. 56, pp. 217-218, Feb. 1968.
(22) F. F. Fang and A. B. Fowler, "Transport properties of electrons in inverted Si surfaces," Phys. Rev., vol. 169, p. 619, 1968.
(23) T. Sato, Y. Takeishi, H. Tango, H. Ohnuma and Y. Okamoto, "Drift velocity saturation of holes in Si inversion layers," J. Phys. Soc. Japan, vol. 31, pp. 1846-1847, 1971.
(24) F. N. Trofimenkoff, "Field-dependent mobility analysis of the field-effect transistor," Proc. IEEE, vol. 53, p. 1765-1766, 1965.
(25) H. C. Pao and C. T. Sah, "Effect of diffusion current on characteristics of metal-oxide (insulator) -semiconductor transistors," Solid-State Electronics, vol. 9, p. 927, 1966.
(26) Y. Hayashi and Y. Tarui, "Exponential current in MOST-type devices and deterioration of reverse current in p-n junctions ," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 67-6, 1967.
(27) M. B. Barron, "Low-level currents in insulated-gate field-effect transistors," Solid-State Electronics, vol. 15, p. 293, 1972.
(28) R. R. Troutman, "Subthreshold design considerations for insulated-gate field-effect transistors," 1973 ISSCC Digest of Tech. Papers, Feb. 1973.

(29) R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," IEEE J. Solid-State Circuits, vol. SC-7, p. 146-153, Apr. 1972.
(30) T. Masuhara, J. Etoh and M. Nagata, "A MOSFET model including low-current region near threshold," Trans. IECE Japan, vol. 56-C, p. 496, 1973.
(31) T. Masuhara, J. Etoh and M. Nagata, "A precise MOSFET model for low-voltage circuits," IEEE Trans. Electron Devices, vol. ED-21, pp. 363-371, June 1974.
(32) T. Masuhara, J. Etoh and M. Nagata, "A MOSFET model including low-current region near threshold," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 72-56, Mar. 1973.
(33) C. T. Sah and H. C. Pao, "The effects of fixed bulk charge on the characteristics of metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol. ED-13, pp. 393-409, Apr. 1966.
(34) G. Merckel, J. Borel and N. Z. Cupcea, "An accurate large-signal MOS transistor model for use in computer-aided design," IEEE Trans. Electron Devices, vol. ED-19, pp. 681-690, May 1972.
(35) J. R. Brews, "Carrier-density fluctuations and the IGFET mobility near threshold," J. Appl. Phys., vol. 46, pp. 2193-2203, May 1975.
(36) H. F. Wolf, "Silicon semiconductor data," New York: Pergamon Press, 1969.
(37) K. G. Aubuchon, Presented at the International Conference on Properties and Use of MIS Structures, Grenoble, France, 1969.
(38) P. J. Coppen, K. G. Aubuchon, L. O. Bauer and N. E. Mover, Solid-State Electronics, vol. 15, p. 165, 1972.
(39) T. W. Sigmon and R. Swanson, "MOS threshold shifting by ion-implantation," Solid-State Electronics, vol. 16, p. 1217, 1973.

(40) S. D. Brotherton and P. Burton, "The influence of non-uniformly doped substrates on MOS C-V curves," Solid-State Electronics, vol. 13, p. 1591, 1970.
(41) T. Tanaka, "Shift of the gate threshold voltage of MOS transistors due to the induction of shallow impurities," J. Appl. Phys. Japan, vol. 10, p. 84, 1971.
(42) M. R. MacPherson, "Threshold shift calculations for ion-implanted MOS devices," Solid-State Electronics, vol. 15, p. 1319, 1972.
(43) T. Warabisako, I. Yoshida and T. Tokuyama, "Properties of MOS structures prepared on substrates having ion-implanted impurity distribution profile," Proc. 4th Conf. Solid-State Devices, Tokyo, 1972.
(44) R. A. Moline and G. W. Reutlinger, "Self-aligned maskless chan stops for IGFET integrated circuits," IEEE Trans. Electron Devices, vol. ED-20, p. 1129, 1973.
(45) T. Masuhara and J. Etoh, "Control of low-level currents in MOSFET by ion-implantation," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 74-5, Apr. 1974.
(46) T. Masuhara and J. Etoh, "Low-level currents in ion-implanted MOSFET," IEEE Trans. Electron Devices, vol. ED-21, pp. 799-807, Dec. 1974.
(47) T. Masuhara and M. Kubo, "Control and Design of MOSFET low-level currents by ion-implantation," 1974 IEDM Digest of Tech. Papers, Washington D.C., Dec. 1974.
(48) J. Lindhard, M. Schaff and H. E. Schiott, Mat. Fys. Medd. Dan. Vid. Selsk., vol. 33, no. 14, 1963.
For numerical calculation of range and standard deviation, W. S. Johnson and J. F. Gibbons, "Projected range statistics in semiconductors," Stanford University Bookstore.

(49) J. F. Gibbons and S. Mylroie, "Estimation of impurity profiles in ion-implanted amorphous targets using joined-half Gaussian distributions," Appl. Phys. Lett., vol.22, p. 568, 1973.
And,
S. Mylroie and J. F. Gibbons, "Comparison of third central moments for projected range distributions of common ion-implanted dopants in silicon," Proc. 3rd. Conf. on Ion-Implantation, New York, Dec. 1972.
(50) R. Lindner, Bell System Tech. J., vol. 41, p. 803, 1962.
(51) J. R. Edwards and G. Marr, "Depletion-mode IGFET made by deep ion-implantation," IEEE Trans. Electron Devices, vol. ED-20, p. 283, 1973.
(52) K. Nakanuma and M. Kamoshida, J. Appl. Phys., vol. 45, p. 334, 1974.
(53) W. Schmmert, L. Gabler and H. Hoefflinger, "Sub-threshold and active region characterization of ion-implanted buried-channel MOS transistors," 1974 Intl. Electron Devices Meeting Digest of Tech.Papers, Washinton D.C., Dec. 1974.
(54) H. J. Sigg, G. D. Vandelin, T. P. Cauge and J. Kocsis, "D-MOS transistor for microwave applications," IEEE Trans. Electron Devices, vol. ED-19, pp. 45-53, 1972.
(55) Y. Tarui, Y. Hayashi and T. Sekigawa, "Diffusion self-aligned MOST: A new approach for high speed device," Proc. 1st. Conf. Solid-State Devices, Tokyo, 1969.
(56) Y. Tarui et al., "Diffusion self-aligned enhancement-depletion MOSIC," Proc. 2nd. Conf. Solid-State Devices, Tokyo, 1970.
(57) T. J. Rodgers and J. D. Meindl, "VMOS: High-speed TTL compatible MOS logic," IEEE J. Solid-State Circuits, vol. SC-9, pp. 239-249, Oct. 1974.
(58) K. Ohta et al., "A high speed logic LSI using diffusion self-aligned enhancement-depletion MOSIC," IEEE J. Solid-State Circuits, vol. SC-10, pp. 314-321, 1975.

(59) H. Masuda, T. Masuhara, M. Nagata and N. Hashimoto, "Device design of E/D gate MOSFET," Proc. 4th. Conf. Solid-State Devices, Tokyo, 1972.
(60) T. J. Rodgers, S. Asai, M. D. Pocha, R. W. Dutton and J. D. Meindl, "DMOS experimental and theoretical study," 1975 ISSCC Digest of Tech. Papers, Philadelphia Pa., Feb. 1975.
(61) H. C. Lin and W. N. Jones, "Computer analysis of the double diffused transistor for integrated circuits," IEEE Trans. Electron Devices, vol. ED-20, pp. 275-283, 1973.
(62) T. Sekigawa, Y. Hayashi and Y. Tarui, "Static characteristics of DSA-MOS transistor," Trans. IECE Japan, vol. 58-C, pp. 509-515, 1975.
(63) D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," Proc. IEEE, pp. 2192-2193, Dec. 1967.

REFERENCES FOR CHAPTER 4

(1) J. Macdougall and K. Manchester, Electronics, pp. 86-90, June 1970.
(2) T. Masuhara and M. Nagata, "N-channel MOS integrated circuits using depletion mode load elements," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 70-8, May 1970.
(3) M. Nagata, N. Hashimoto and T. Masuhara, "Nanosecond n-channel monolithic integrated circuits with depletion-mode transistors as load devices," Presented at 1970 Intl. Electron Devices Meeting, Washington D.C., Oct. 1970.
(4) H. C. Lin and C. J. Varker, "Normally-on load devices for IGFET switching circuit," NEREM Rec., pp. 124-125, 1969.
(5) Y. Tarui, Y. Hayashi and T. Sekigawa, "DSA enhancement/ depletion MOSIC," Presented at 1970 Intl. Electron Devices Meeting, Washington D.C., Oct. 1970.

(6) L. Forbes, "N-channel ion-implanted enhancement/depletion FET circuit and fabrication technology," IEEE J. Solid-State Circuits, vol. SC-8, pp. 226-230, June 1973.
(7) T. Masuhara, M. Nagata and N. Hashimoto, "A high performance n-channel MOSLSI using depletion-type load elements," IEEE J. Solid-State Circuits, vol. SC-7, pp. 224-231, June 1972. This paper was presented at 1971 ISSCC, Philadelphia, Pa., Feb. 1971.
(8) S. Nishimatsu and T. Tokuyama, "N-channel enhancement type MOSICs utilizing alumina film," Proc. 1st. Conf. Solid-State Devices, Tokyo, 1969.
(9) N. Hashimoto, M. Nagata and T. Masuhara, "Technology and performance of n-channel MOSLSIs using depletion-type load elements," Proc. 3rd. Conf. Solid-State Devices, Tokyo, 1971.
(10) S. Nishimatsu, N. Hashimoto, T. Masuhara and M. Nagata, "Stability investigation of n-channel MOSFET utilizing alumina film for large scale dynamic memory array," Proc. 5th. Conf. Solid-State Devices, Tokyo, 1973.
(11) T. Masuhara, Y. Adachi, M. Nagata and N. Hashimoto, "Low voltage dynamic MOS memory," Trans. IECE Japan, vol. 57-C, pp. 271-278, Aug. 1974.
(12) J. D. Schmidt, "Integrated MOS random access memory," Solid-State Design, p. 21, Jan. 1965.
(13) D. Lund, C. Allen, S. Anderson and G. Tu, "Design of a megabit semiconductor memory system," AFIPS Fall Joint Computer Conf. Proc., p. 53, Dec. 1970.
(14) W. M. Regitz and J. Karp, "A three transistor cell 1024 bit 500 ns MOSRAM," 1970 ISSCC Digest of Tech. Papers, p. 42, Philadelphia, Pa., Feb. 1970.
(15) R. H. Dennard, "Field-effect transistor memory," U.S. Patent 3387286, June 4, 1968.
(16) S. Sato, M. Katsueda et al., "HICAD-1: A general purpose circuit analysis system," Natl. Conv. IECE Japan, 1970.

(17) A. K. Rapp, 1969 ISSCC Digest of Tech. Papers, Philadelphia, Pa., Feb. 1969.
(18) Y. Hayashi et. al., "Design theory of ED-MOS-IC," Trans. IECE Japan, vol. 55-C, p.337, July 1972.
(19) Y. Hayashi et. al., "Design of ED-MOS buffer," Trans. IECE Japan, vol. 55-C, p. 520, Oct. 1972.

REFERENCES FOR CHAPTER 5

(1) A. K. Rapp, L. P. Wennick, H. Borkan and K. R. Keller, "Complementary MOS integrated binary counter," 1967 ISSCC Digest of Tech. Papers, Philadelphia, Pa., Feb., 1967.
(2) R. G. Daniels and R. R. Burgers, "The electronic wrist-watch: An application for Si gate CMOSICs," 1971 ISSCC Digest of Tech. Papers, Philadelphia, Pa., Feb. 1971.
(3) T. Masuhara and R. S. Muller, "Complementary DMOS process for LSI," 1975 Intl. Electron Devices Meeting Digest of Tech Papers, Washington D.C., Dec. 1975.
(4) T. Masuhara and R. S. Muller, "Complementary DMOS process for LSI," IEEE J. Solid-State Circuits, vol. SC-11, pp. 453-458, Aug. 1976.
(5) Y. A. El-Mansy and A. R. Boothroyd, "A simple two-dimensional saturation model of short channel IGFETs for CAD applications, " 1974 Intl. Electron Devices Meeting Digest of Tech. Papers, Washington D.C., Dec. 1975.
(6) J. Tihanyi and H. Schlotterer, "Properties of ESFI MOS transistors due to the floating substrate and the finite volume," 1974 Intl. Electron Devices Meeting Digest of Tech. Papers, Washington D.C., Dec. 1974.
(7) K. Ohta, M. Morimoto, H. Saitoh, F. Fukuta, A. Morino, K. Shimizu, Y. Hayashi and Y. Tarui, "A high speed logic LSI using diffusion-self-aligned enhancement-depletion MOSIC," IEEE J. Solid-State Circuits, vol. SC-10, pp. 314-321, Oct. 1975.

The results of this thesis have been published in the journals as listed below.

CHAPTER 3

(1) T. Masuhara, J. Etoh and M. Nagata, "A MOSFET model including low-current region near threshold," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 72-56, Mar. 1973.
(2) T. Masuhara, J. Etoh and M. Nagata, "A precise MOSFET model for low-voltage circuits," IEEE Trans. Electron Devices, vol. ED-21, pp. 363-371, June 1974.
(3) T. Masuhara and J. Etoh, "Control of low-level currents in MOSFET by ion-implantation," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 74-5, Apr. 1974.
(4) T. Masuhara and J. Etoh, "Low-level currents in ion-implanted MOSFET," IEEE Trans. Electron Devices, vol. ED-21, pp. 799-807, Dec. 1974.
(5) T. Masuhara and M. Kubo, "Control and design of MOSFET low-level currents by ion-implantation," 1974 Intl. Electron Devices Meeting Digest of Tech. Papers, Washington D.C., Dec. 1974.
(6) T. Masuhara and R. S. Muller, "Analytical technique for the design of DMOS transistors," Proc. 8th Conf. Solid-State Devices, Tokyo, Sep. 1976.

CHAPTER 4

(7) T. Masuhara and M. Nagata, "N-channel MOS integrated circuits using depletion mode load elements," Tech. Group on Semiconductors and Semiconductor Devices IECE Japan, Tech. Rep. SSD 70-8, May 1970.

(8) M. Nagata, N. Hashimoto and T. Masuhara, "Nanosecond n-channel monolithic integrated circuits with depletion mode transistors as load devices," Presented at the 1970 Intl. Electron Devices Meeting, Washington D.C., Oct. 1970.
(9) T. Masuhara, M. Nagata and N. Hashimoto, "A high performance n-channel MOSLSI using depletion-type load elements," IEEE J. Solid-State Circuits, vol. SC-7. pp. 224-231, June 1972.
(10) T. Masuhara, Y. Adachi, M. Nagata and N. Hashimoto, "Low voltage dynamic MOS memory," Trans. IECE Japan, vol. 57-C, pp. 271-278, Aug. 1974.

CHAPTER 5

(11) T. Masuhara and R. S. Muller, "Complementary DMOS process for LSI," 1975 Intl. Electron Devices Meeting Digest of Tech. Papers, Washington D.C., Dec. 1975.
(12) T. Masuhara and R. S. Muller, "Complementary DMOS process for LSI," IEEE J. Solid-State Circuits, vol. SC-11, pp. 453-458, Aug. 1976.